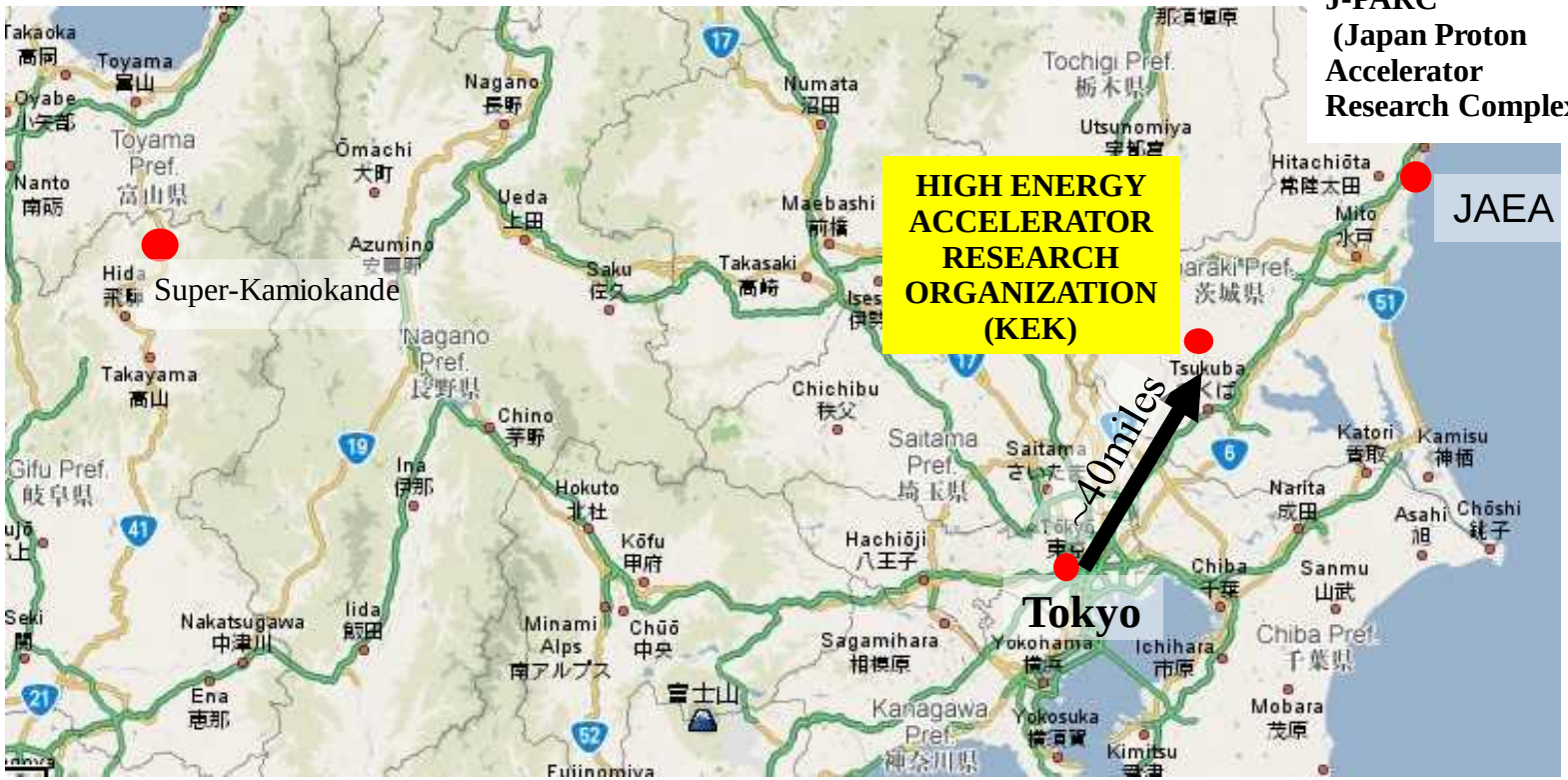
Developments of SOI pixel detectors

Seventh International Meeting on Front-End Electronics
2009/5/18-5/21
Toshinobu Miyoshi (KEK)

4.23 Neutrino beamline
Operation starts

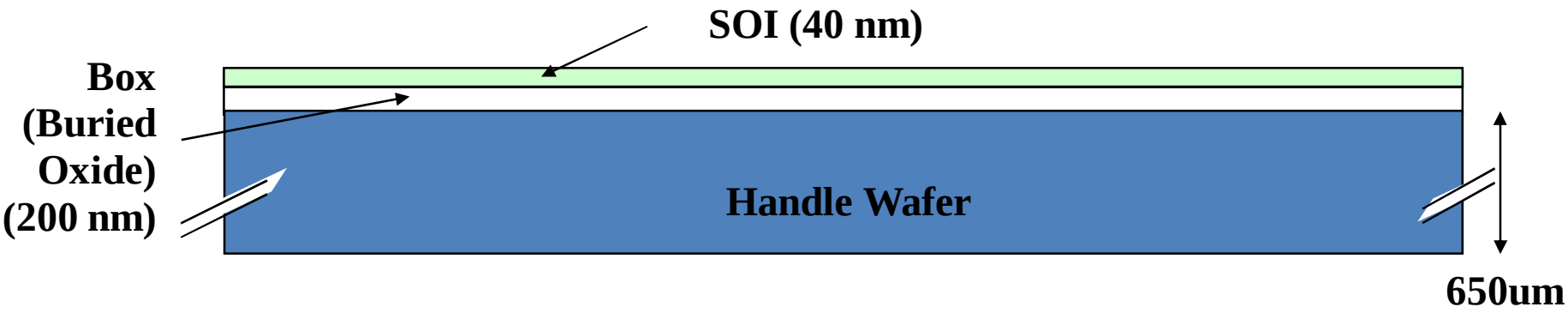


Developments of SOI pixel detector at KEK

- Started as a generic R&D program of KEK Detector Technology Project in 2005.

- aimed at establishing of a SOI Pixel process and developing pixel detectors for many applications.

Silicon-On-Insulator (SOI) pixel detector fabrication

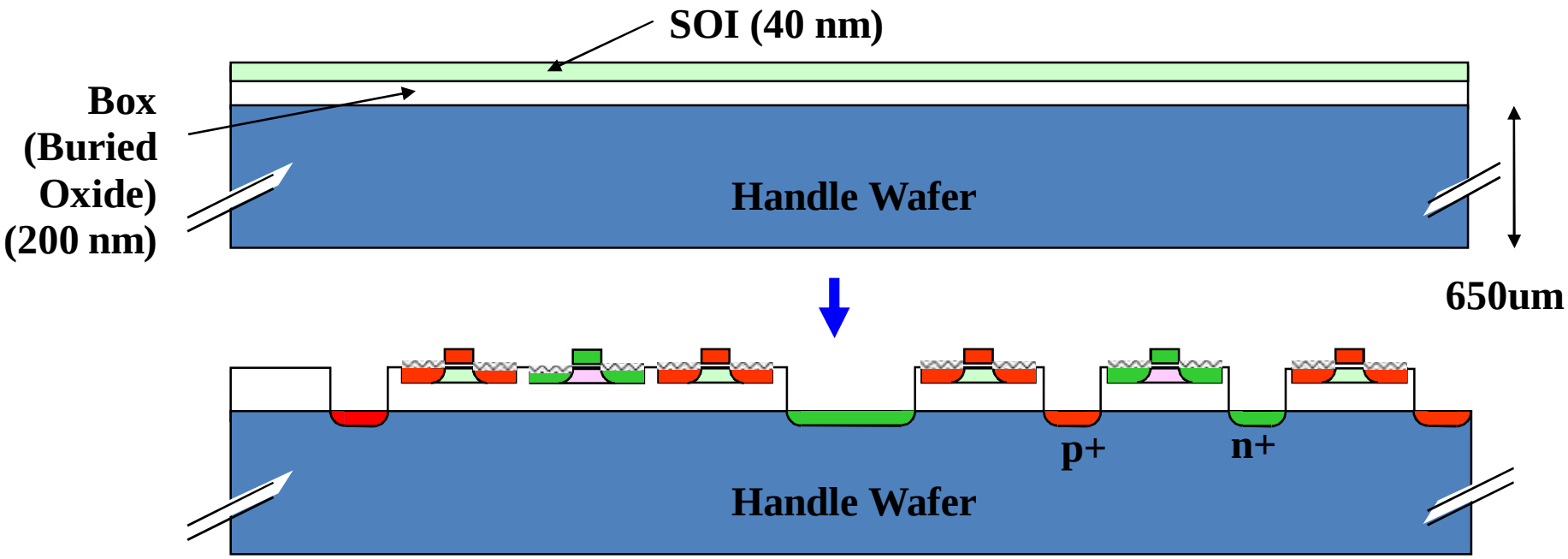


Start from commercial SOI wafer
(e.g.) SOITEC, ShinEtsu
Insulator (buried oxide) between two silicon

High-resistivity silicon = Handle wafer
Use as sensor

Low-resistivity silicon = SOI layer
Use as CMOS transistor formation

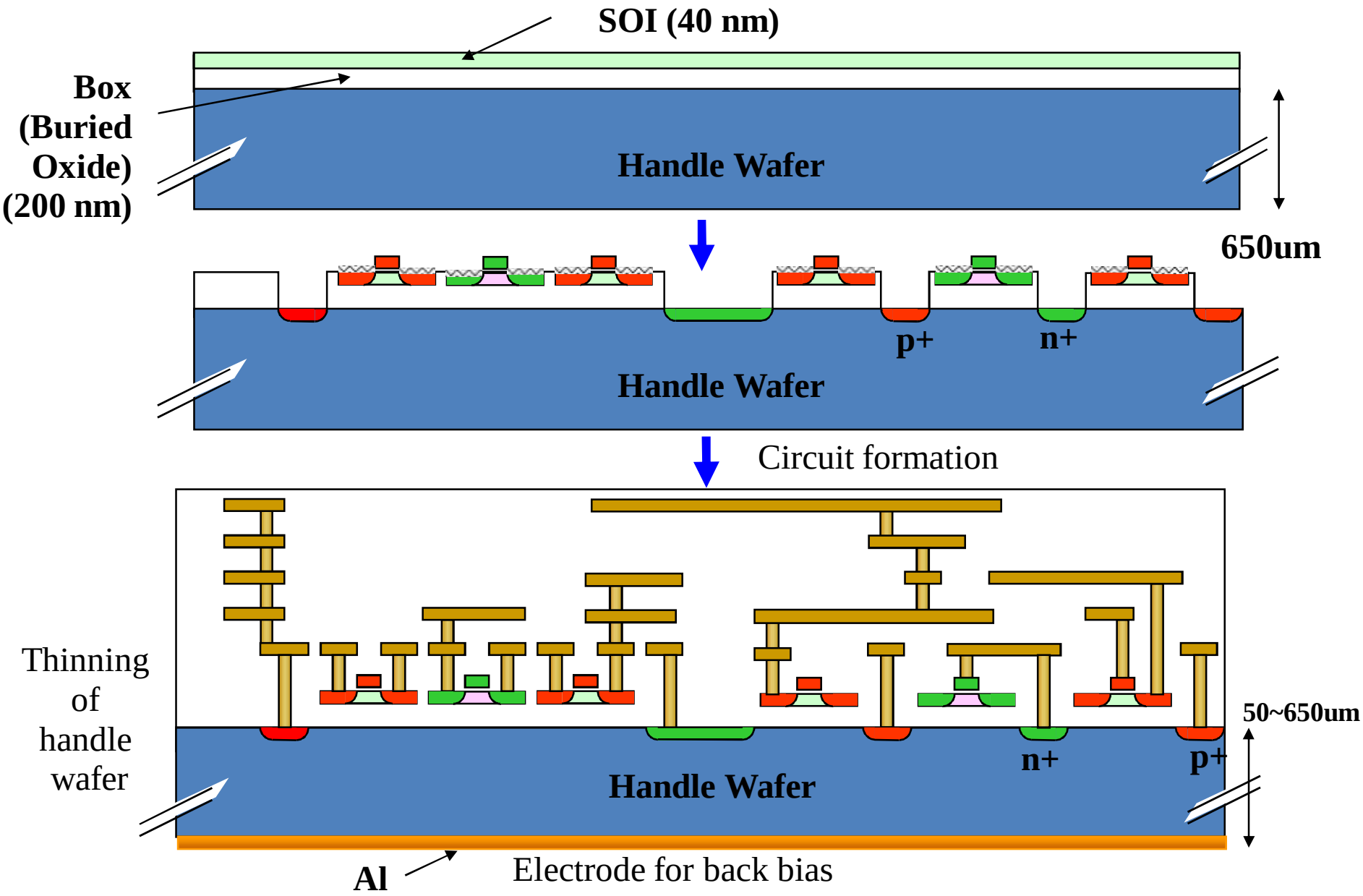
Silicon-On-Insulator (SOI) pixel detector fabrication



Implant p+ to produce pn junction
(handle wafer = n- bulk)

Form MOS transistor on SOI layer

Silicon-On-Insulator (SOI) pixel detector fabrication



Features of SOI Pixel Detector

-Truly monolithic detector (→ High Density, Low material, Thin Device).

-Standard CMOS can be used (→ Complex functions in a pixel).

-No mechanical bonding (→ High yield, Low cost).

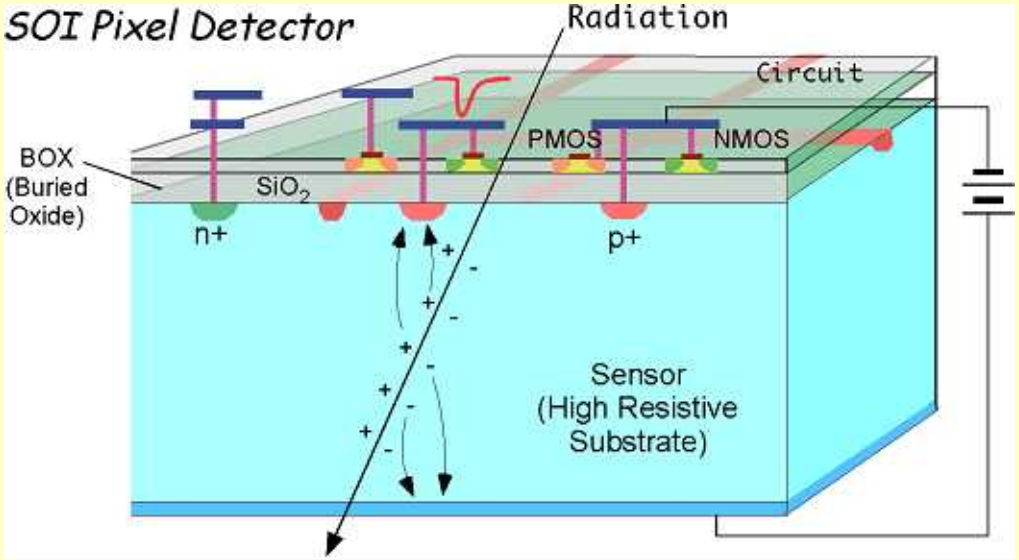
-Fully depleted sensor with small capacitance of the sense node
(→ ~10fF, High conversion gain, Low noise)

-Based on Industrial standard technology (→ Cost benefit and Scalability)

-No Latch Up, Rad Hard.

-Low Power

-Low to High Temp
(4K-300C) operation



History

'05. 7: Start Collaboration with OKI Elec. Co. Ltd.

'05.10: TEG submission to OKI SOI 0.15 um process.

'06.12: 1st 0.15 um MPW run hosted by KEK.

MPW=Multi Project Wafer
(17 designs; KEK, Japanese Universities, LBNL, FNAL, Univ. of Hawaii)

'07.6: Process (and Fab.) has changed from 0.15 um to 0.2 um.

'08.1: 1st 0.2 um (FY07) MPW run was submitted.

'08.6- : SOI chips (FY07) are testing (continue)

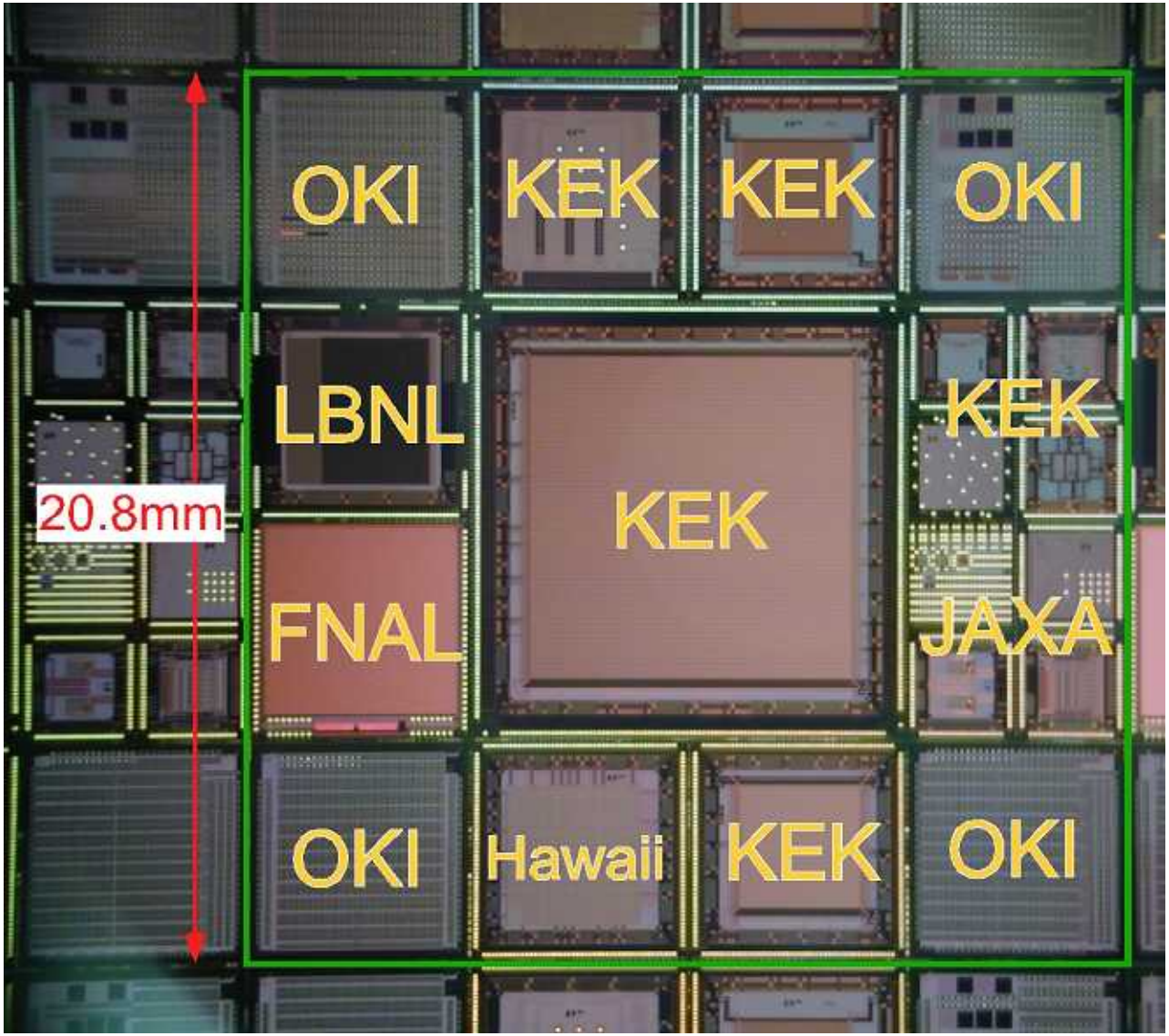
'09.2: 2nd 0.2 um (FY08) MPW run was submitted.

'09.7: 3rd 0.2um (FY09A) MPW run is planned.

OKI 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 4 Metal layers, MIM Capacitor, DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz, ~700 Ω-cm, *n-type*, 650 μm thick
Backside	Thinned to 260 μm Sputtered with Al (200 nm).

KEK SOI MPW run (submitted in Jan. 2008)

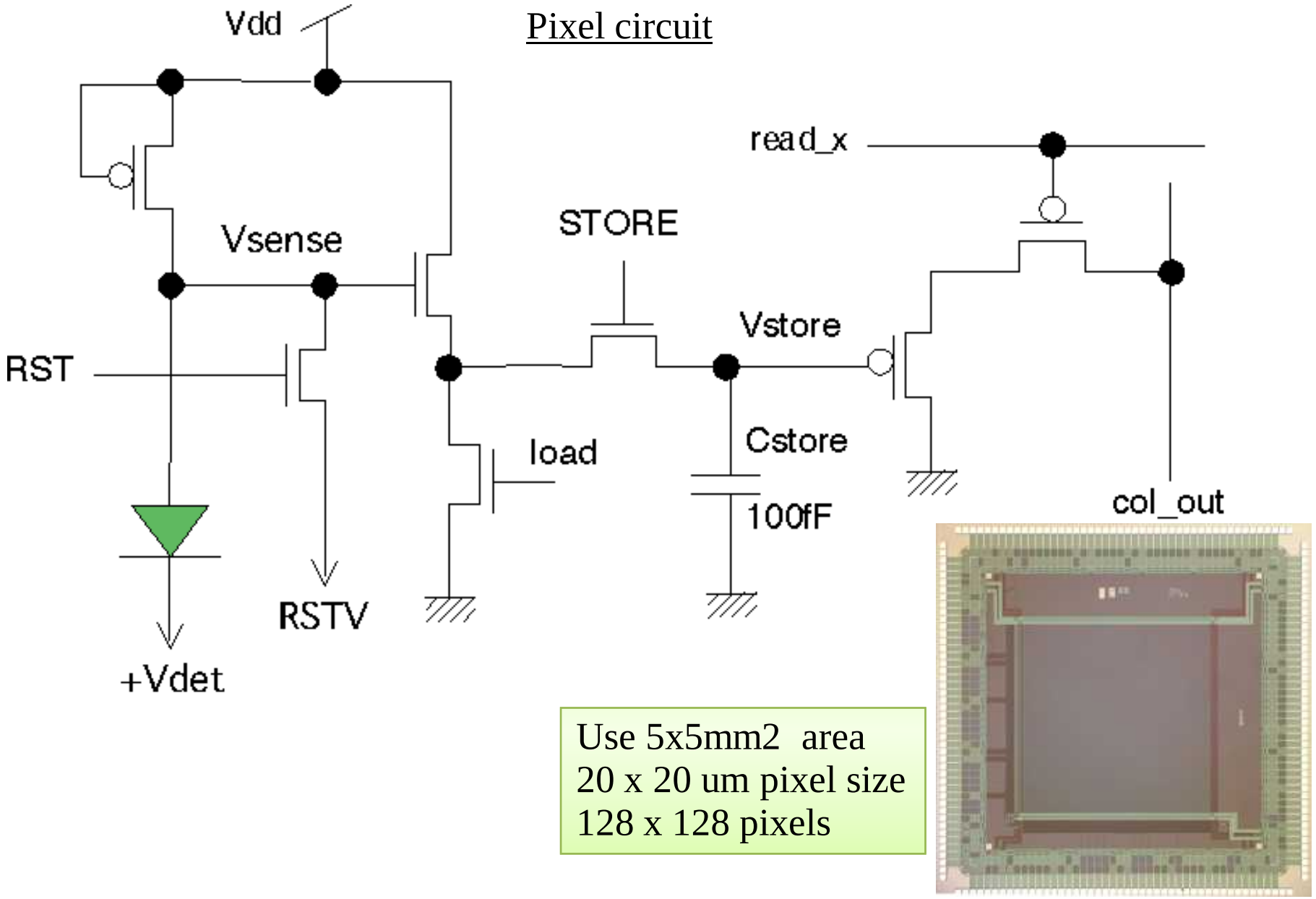


15 designs
KEK(8)
JAXA(4)
(=Japan Aerospace Exploration Agency)
FNAL
LBNL
Hawaii

KEK TEGs (5)
-Sensor characteristics

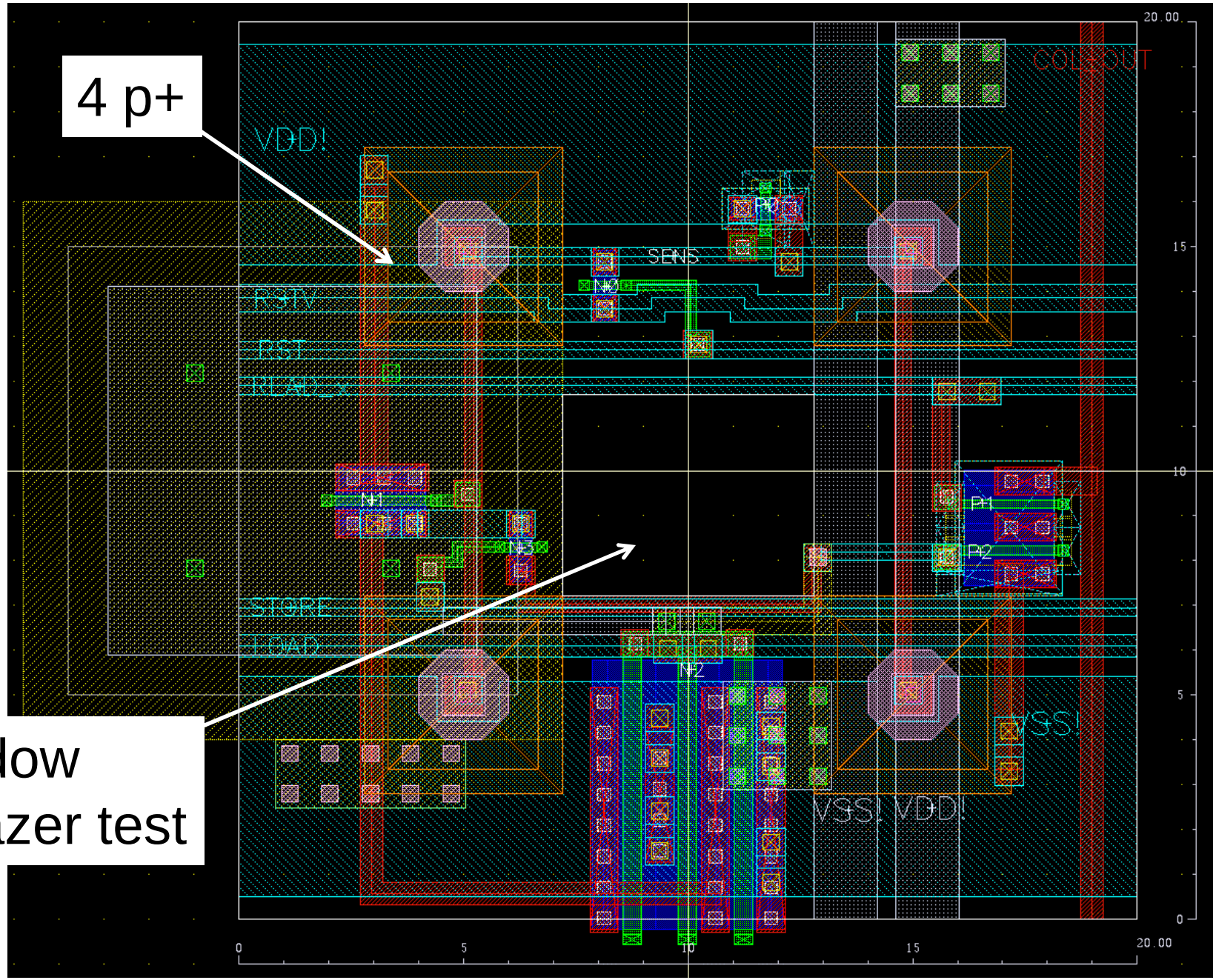
KEK pixel detectors:
INTPIX2
CNTPIX2
SBPIX
-circuit test
-light & X-ray response

Integration Type Pixel (INTPIX2)

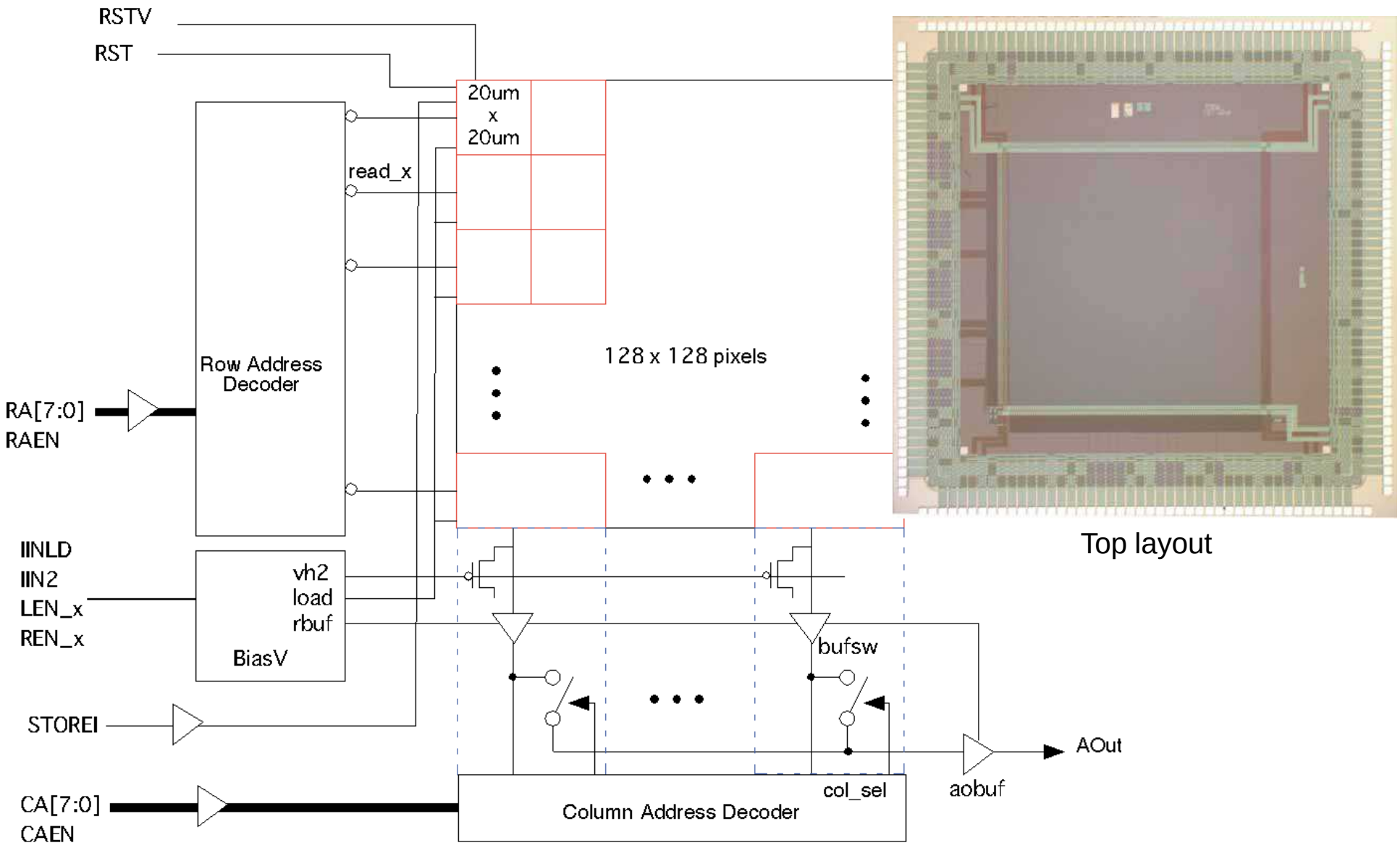


Use 5x5mm2 area
20 x 20 um pixel size
128 x 128 pixels

INTPIX2 pixel layout (20 by 20 um pixel size)



INTPIX2 block diagram & top layout

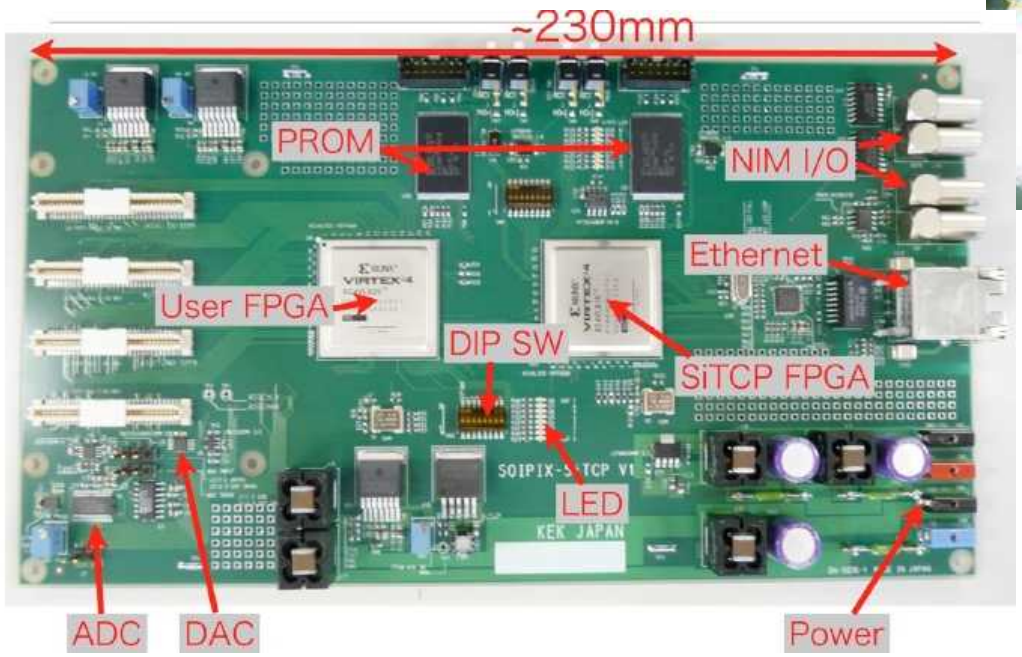


Top layout

INTPIX2 DAQ system

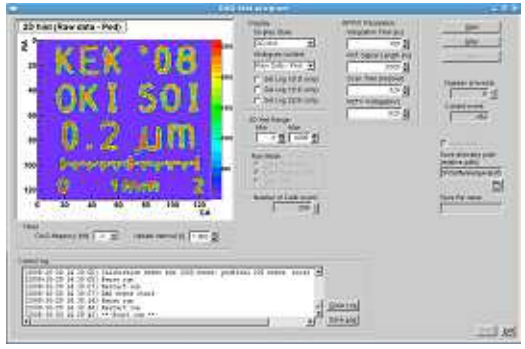
SEABAS=Soipix EvAluation BoArd with SiTCP

INTPIX2
sub-board



ethernet

Mobile PC



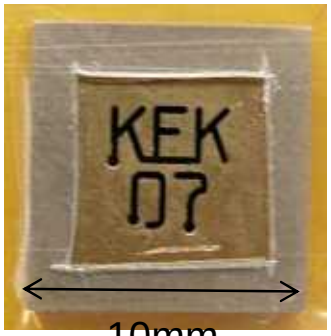
ROOT GUI software

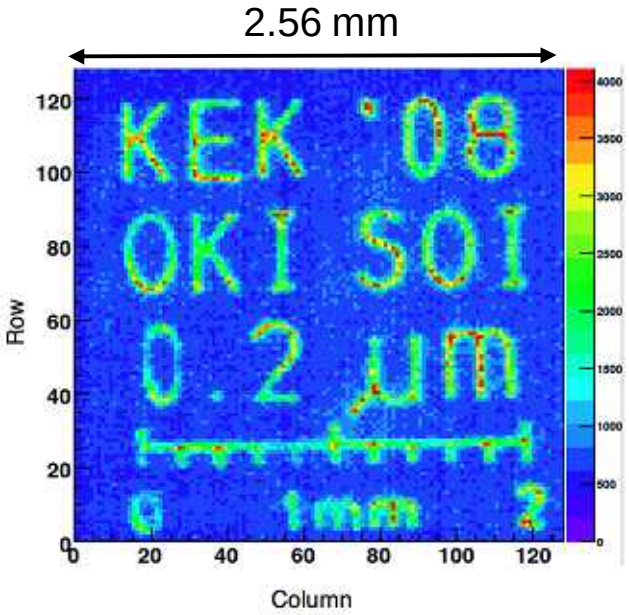
-packaged chip is mounted on sub-board
-Use on-board 12-bit ADC
-User FPGA controls INTPIX2
-SiTCP(network processor) for TCP-IP
-light weight detector system (portable)

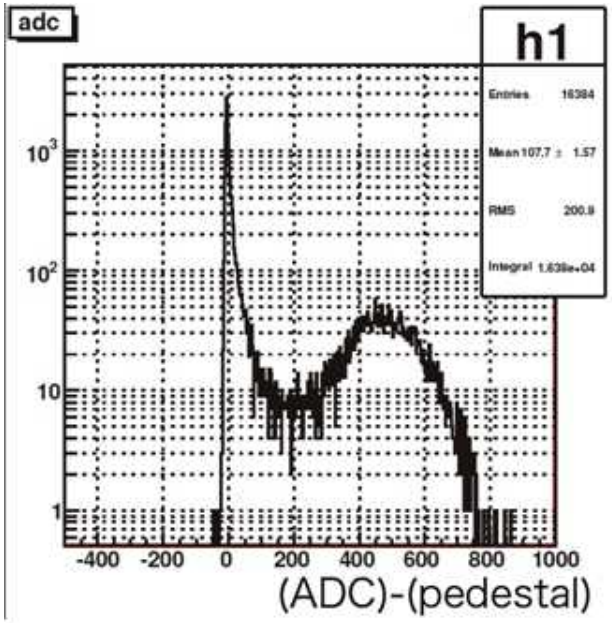
INTPIX2 Images

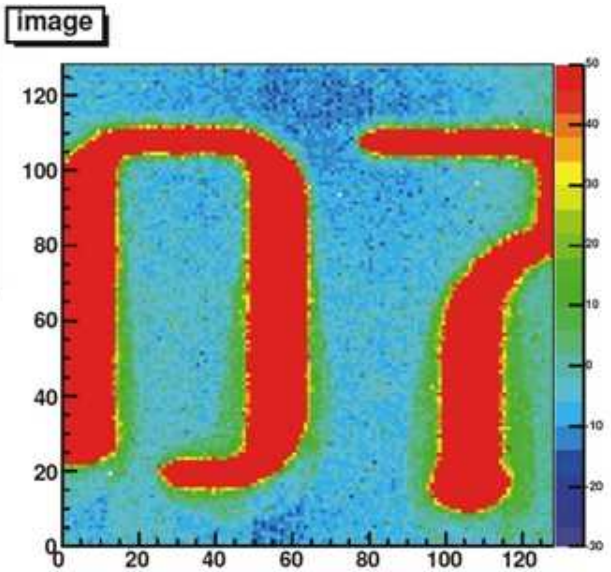
Lazer image
with plastic mask

X-ray image
with metal mask



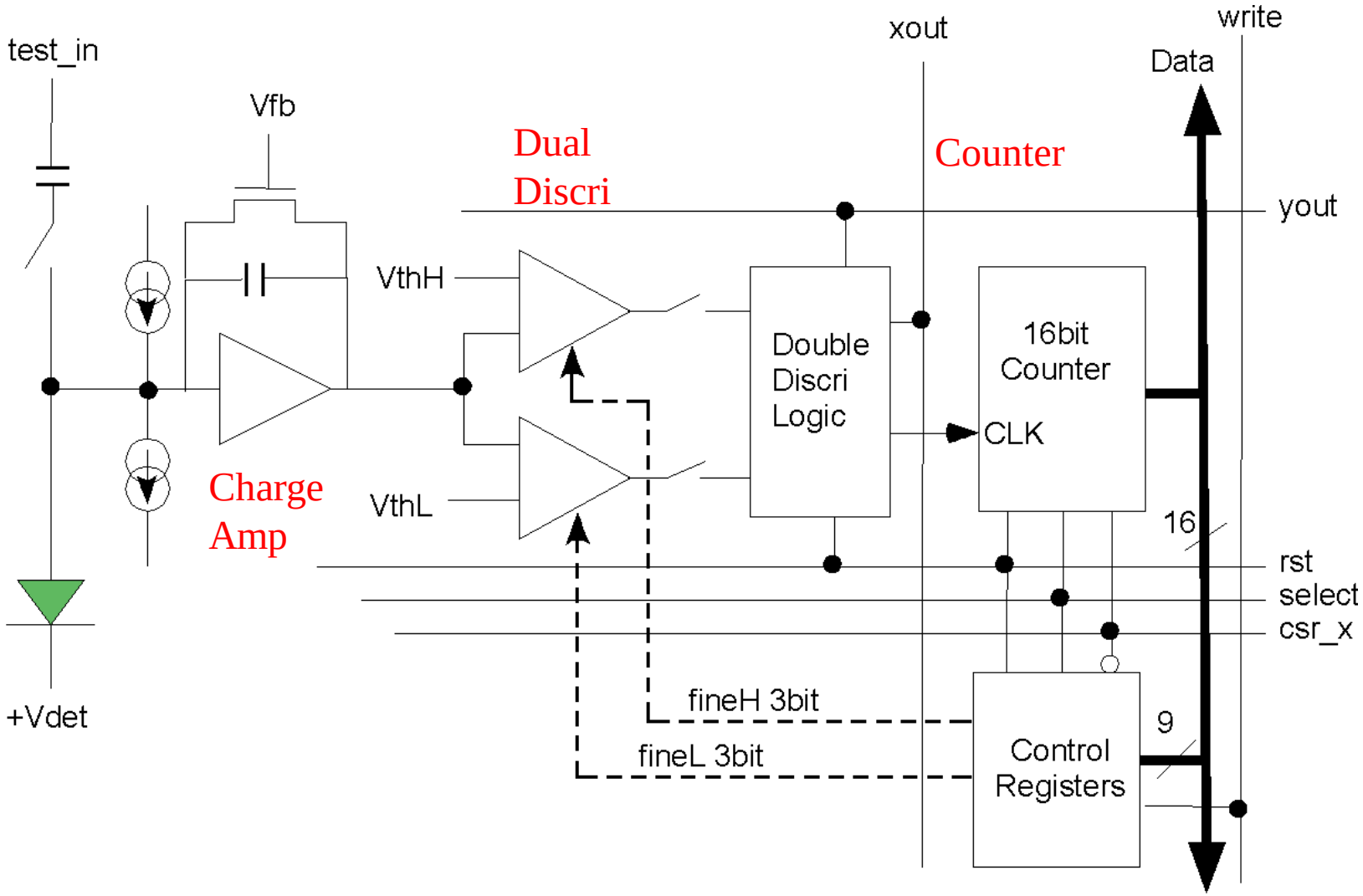






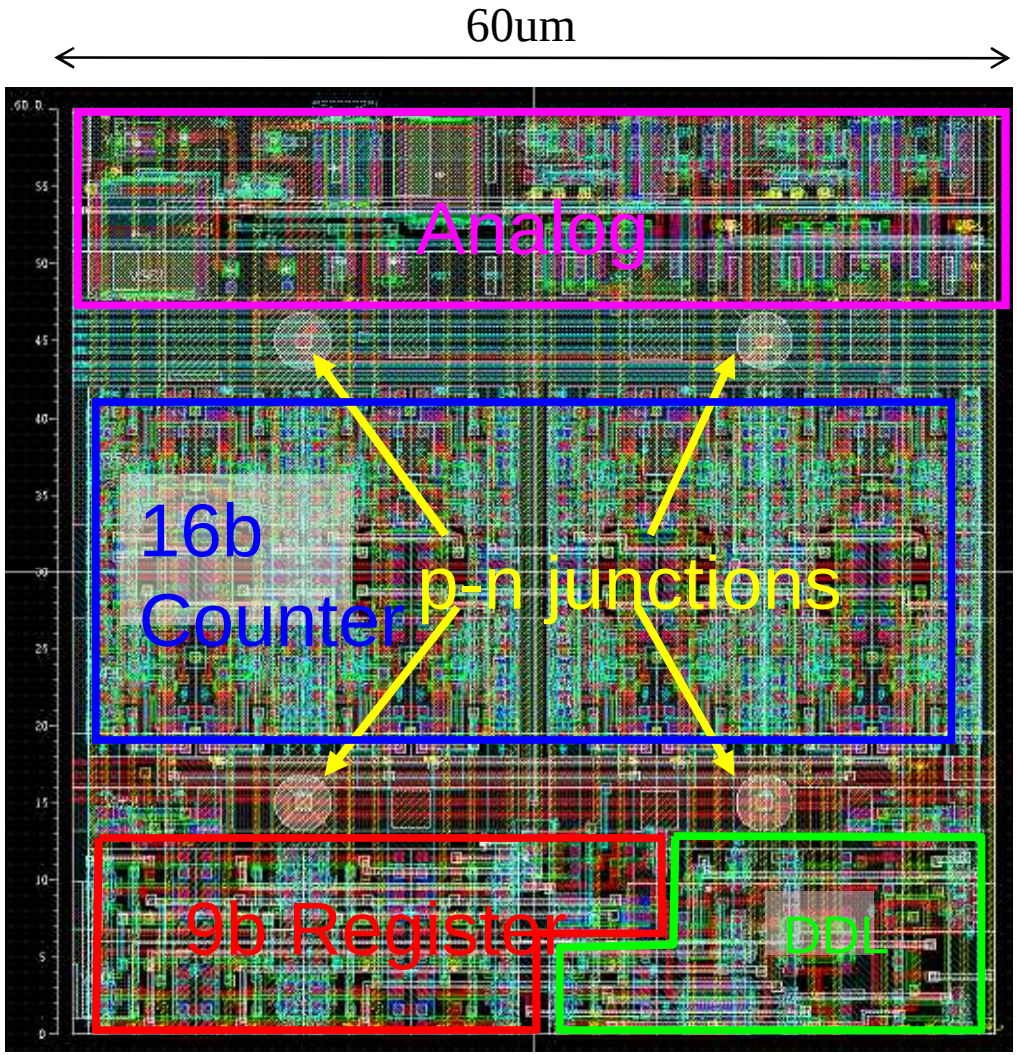
Laser and X-ray response are confirmed

Counting Type Pixel (CNTPIX2)

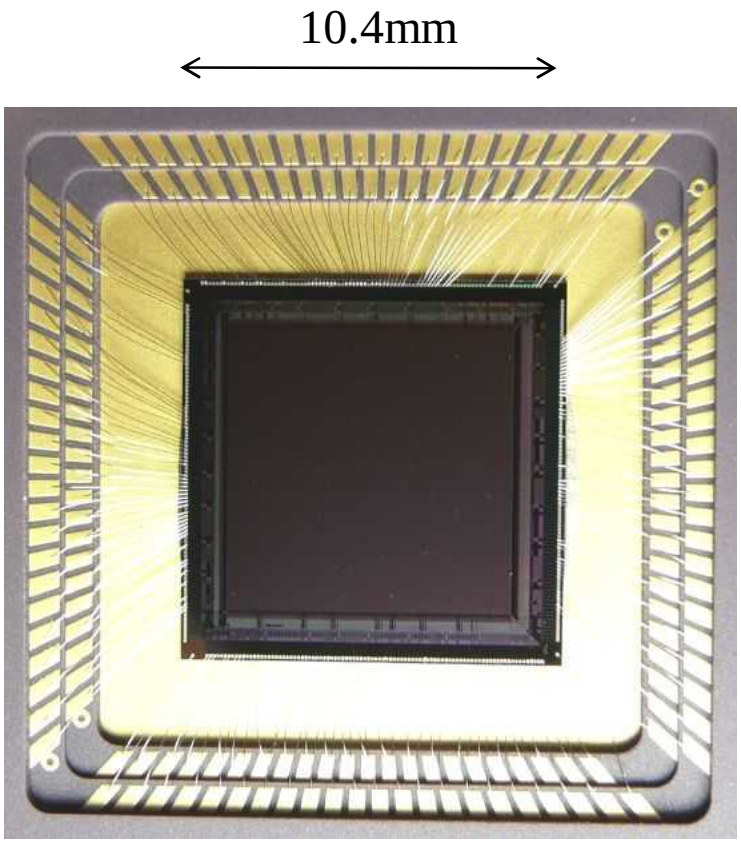


Energy window and counting in each pixel.

CNTPIX2 pixel layout and photograph

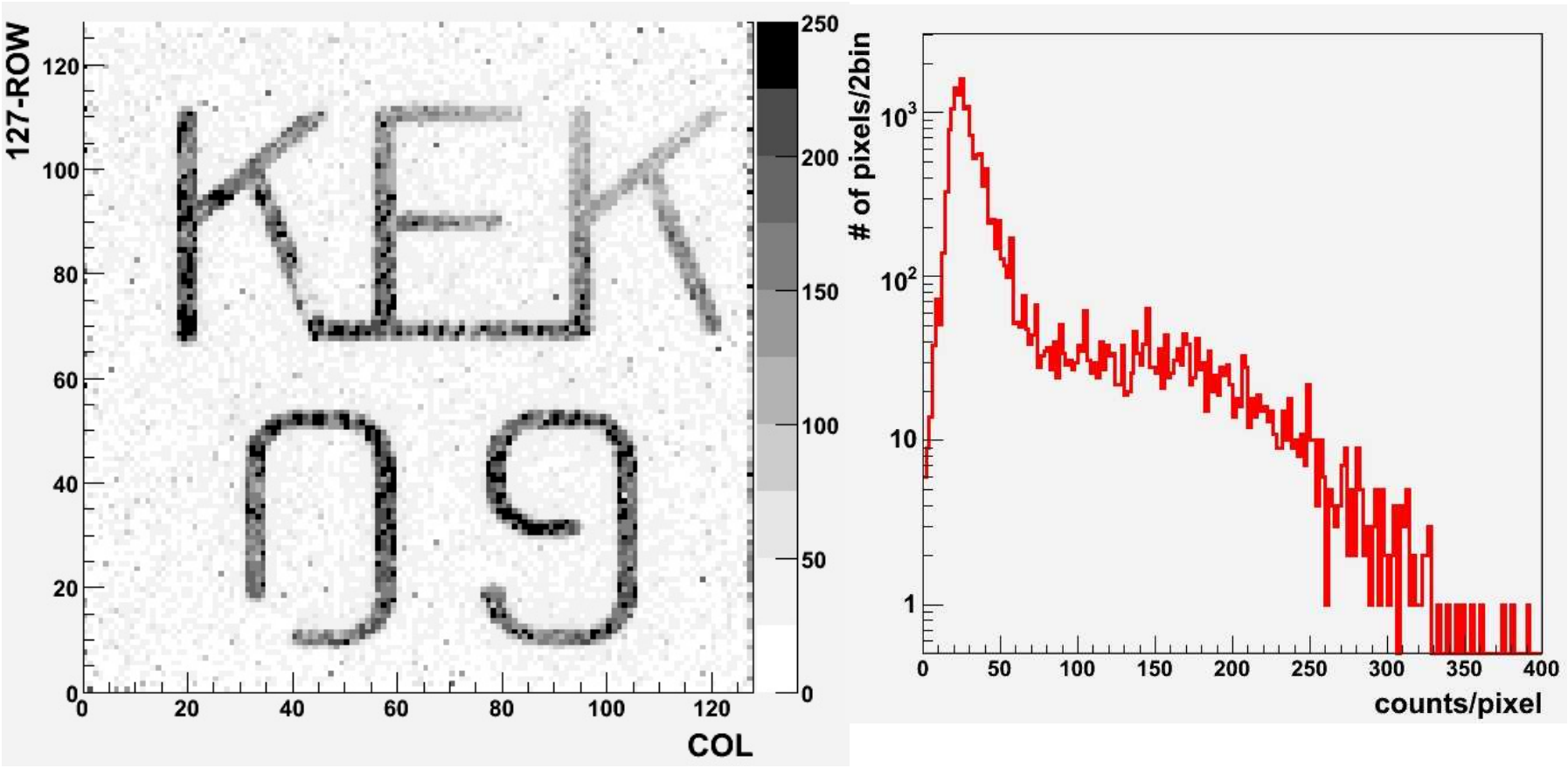


One pixel : ~600 transistors



128 x 128 pixels

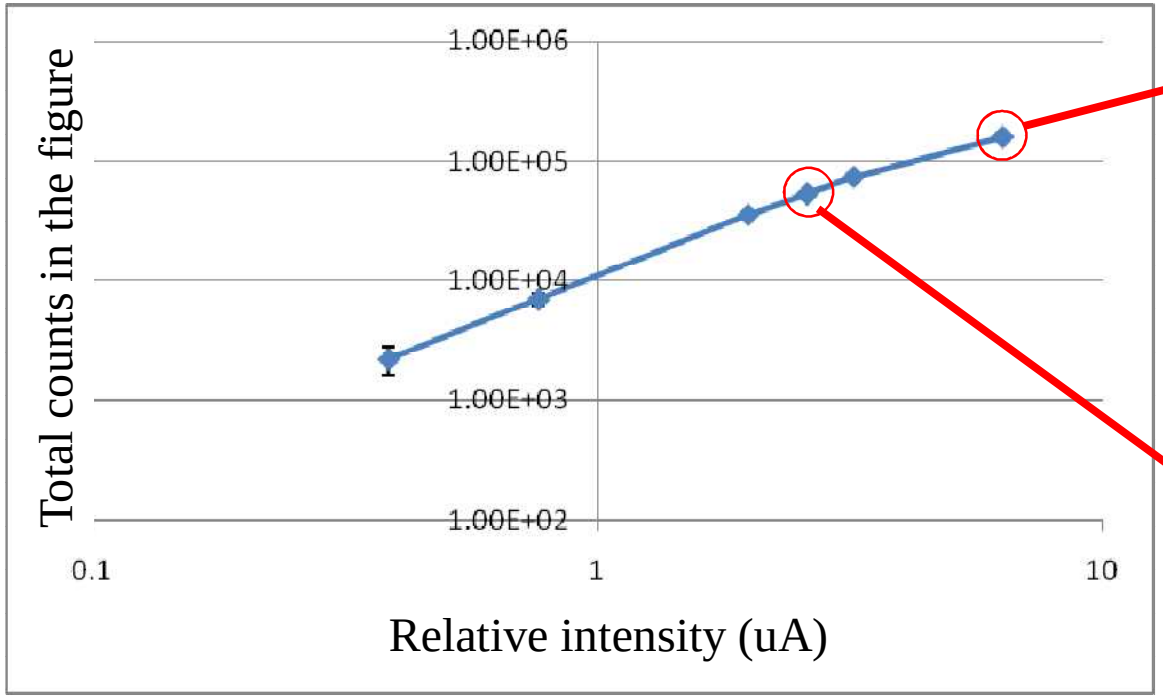
Laser image with metal mask

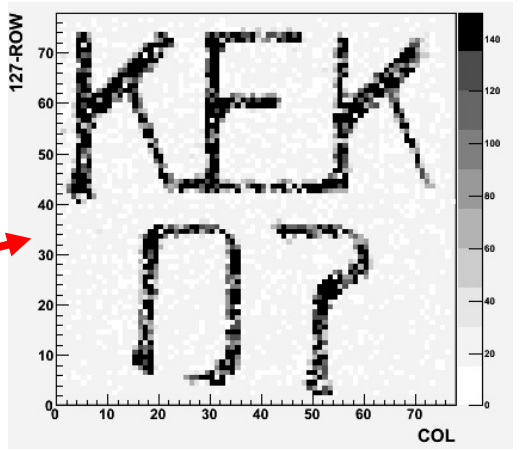


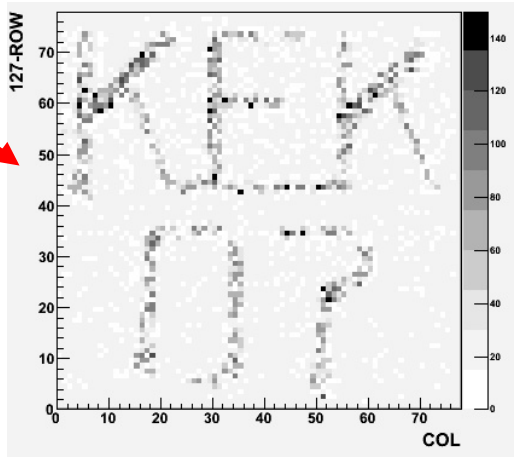
Integration time 1.6ms
Vback =20V, Vth=200mV

Counter works

X-ray sensitivity







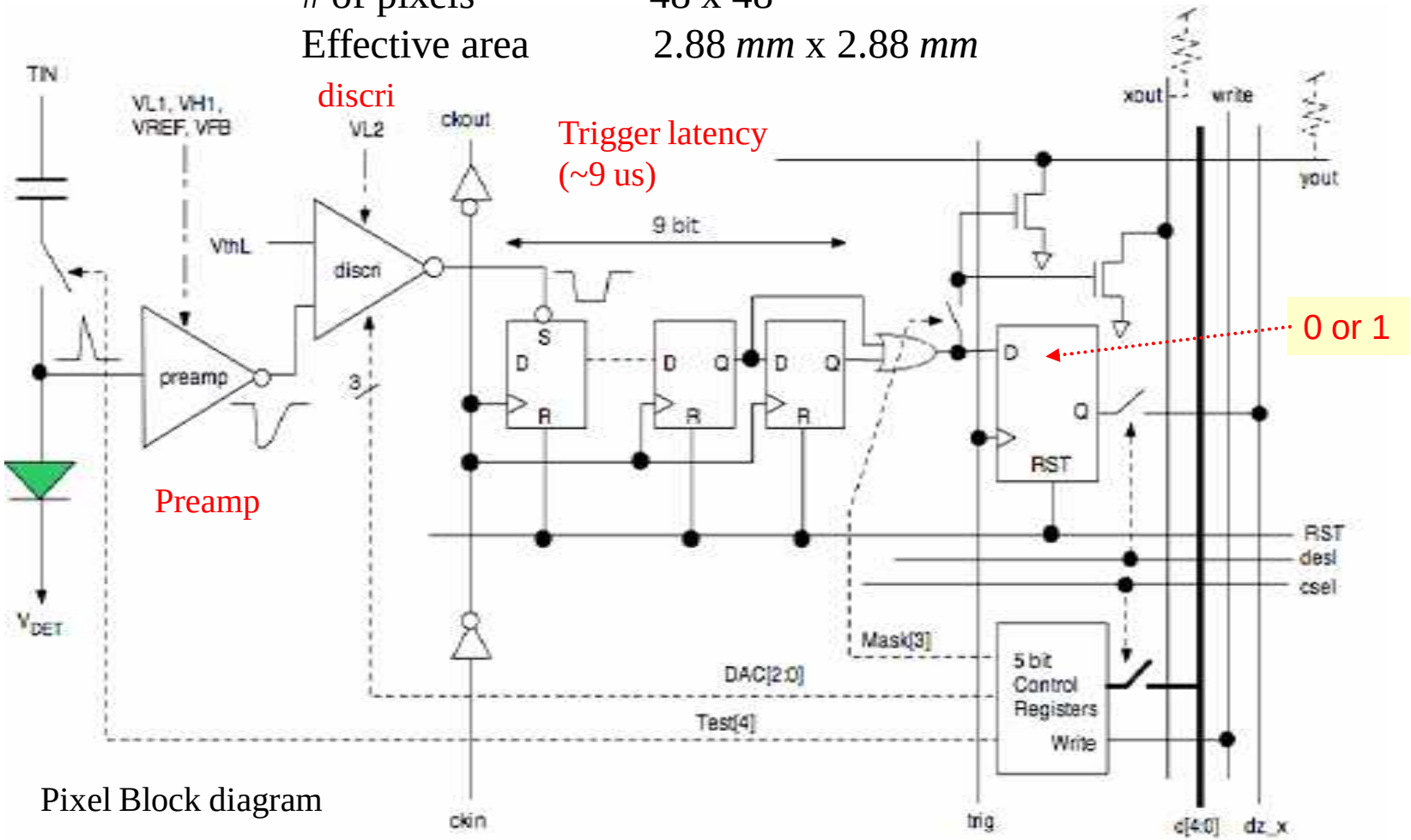
X-ray tube Cu Kalpha 8keV
Photodiode was used for intensity measurement

Total counts increase with intensity

SuperBelle (→Belle II) pixel : SBPIX1

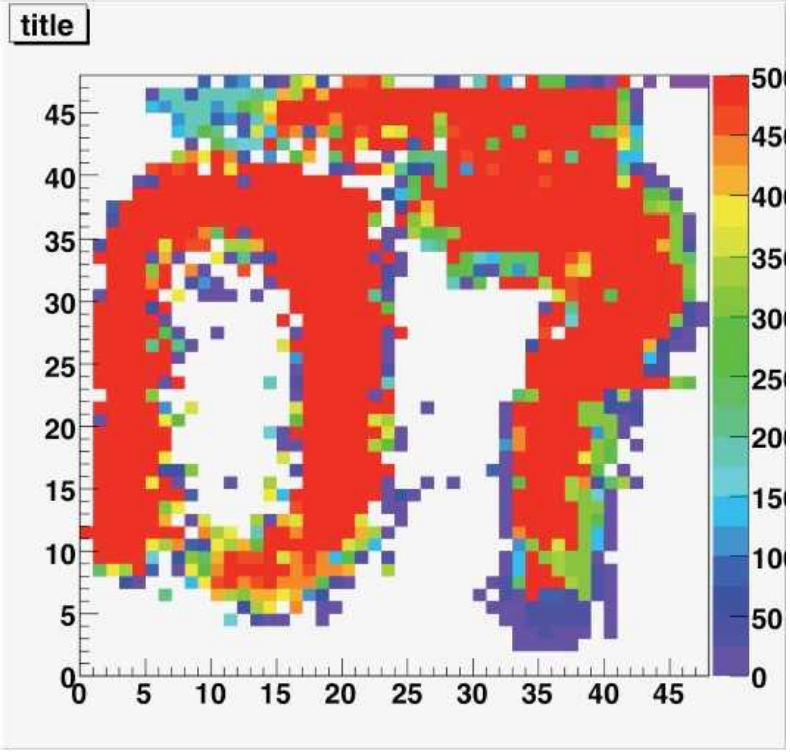
Aimed at application of pixel detector to Belle upgrade

Pixel size	60 *um* x 60 *um*
# of pixels	48 x 48
Effective area	2.88 *mm* x 2.88 *mm*



Pixel Block diagram

SBPIX1 laser image with metal mask



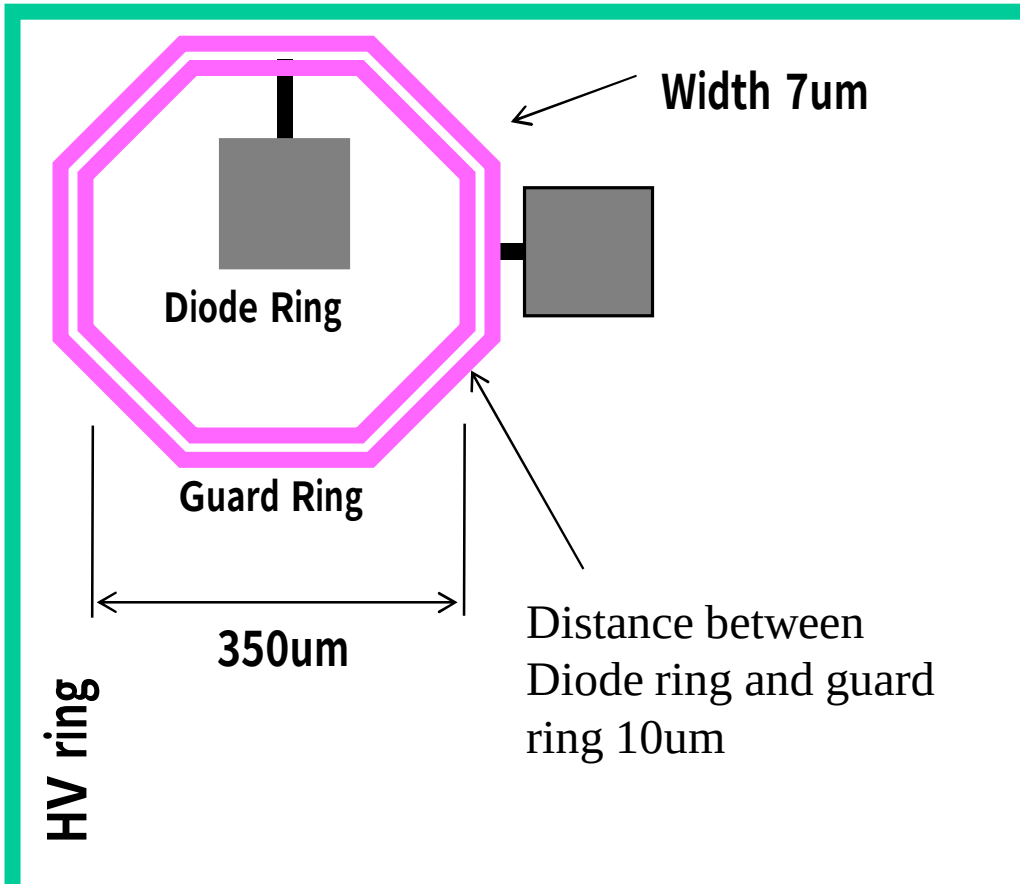
50 event integration

Chip works

Continue R&D

Pixel size 60um → 50um or less

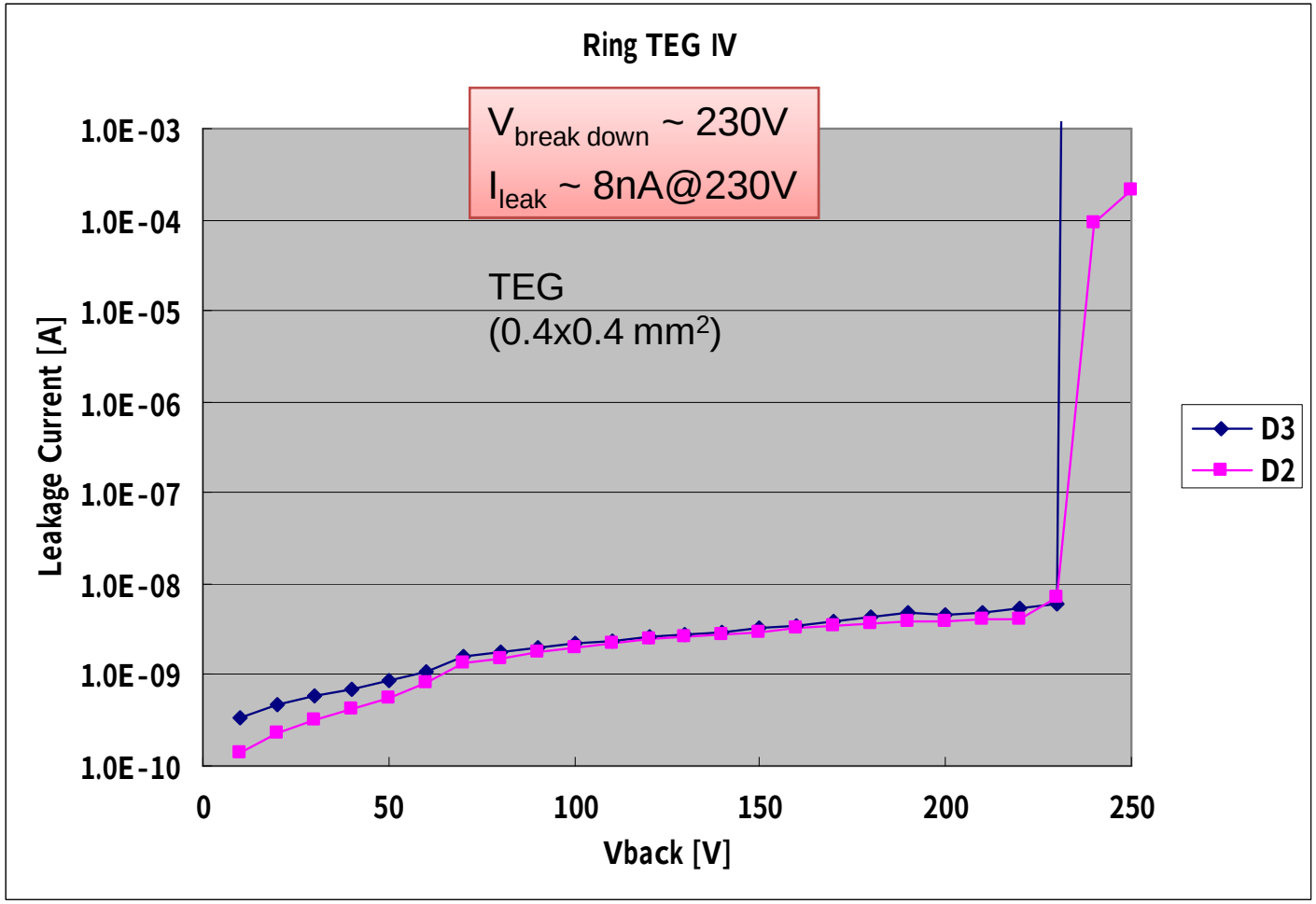
RingTEG



Miyake (Tsukuba Univ.)
Kouriki (KEK)
Ikegami (KEK)

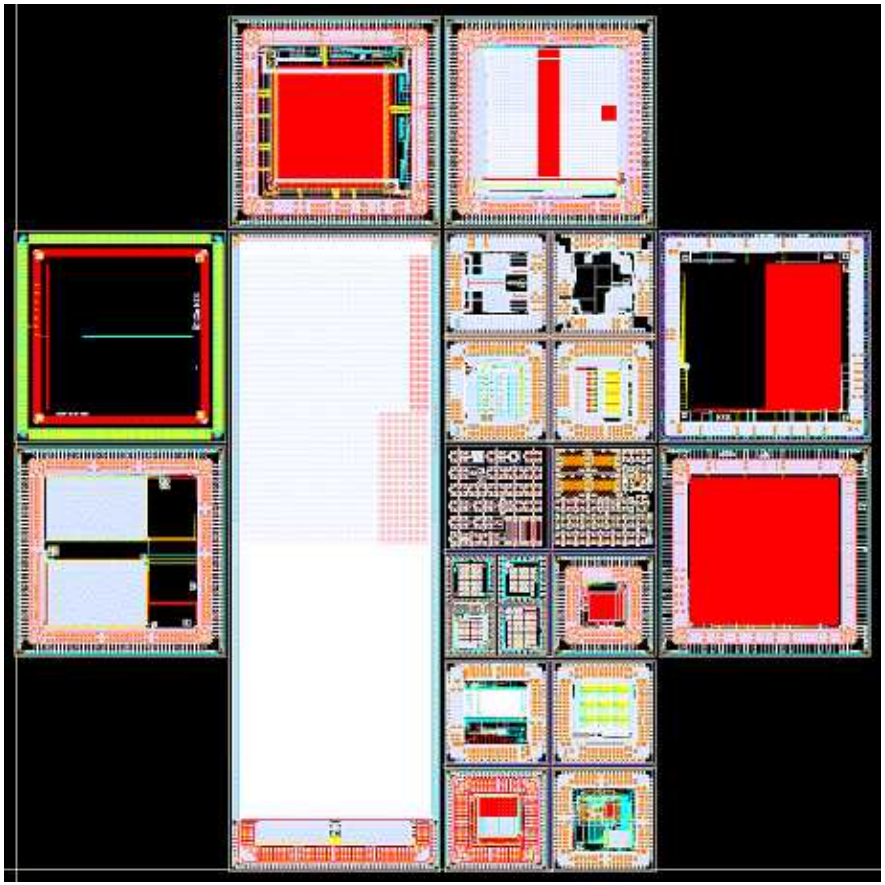
Invastigate relationship between guard ring shape and breakdown voltage

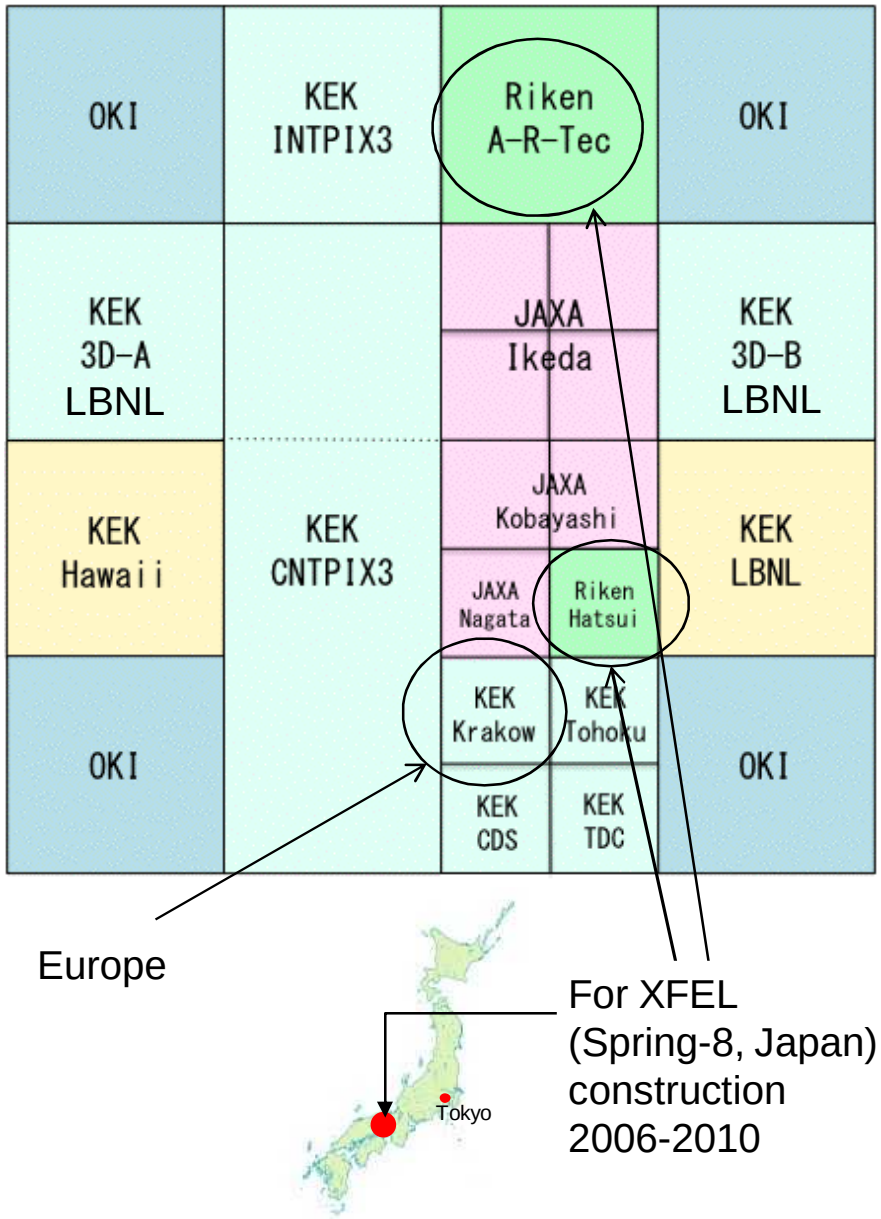
Break Down Voltage & Leak Current



Break Down Voltage can be ~230V with proper guard ring design.

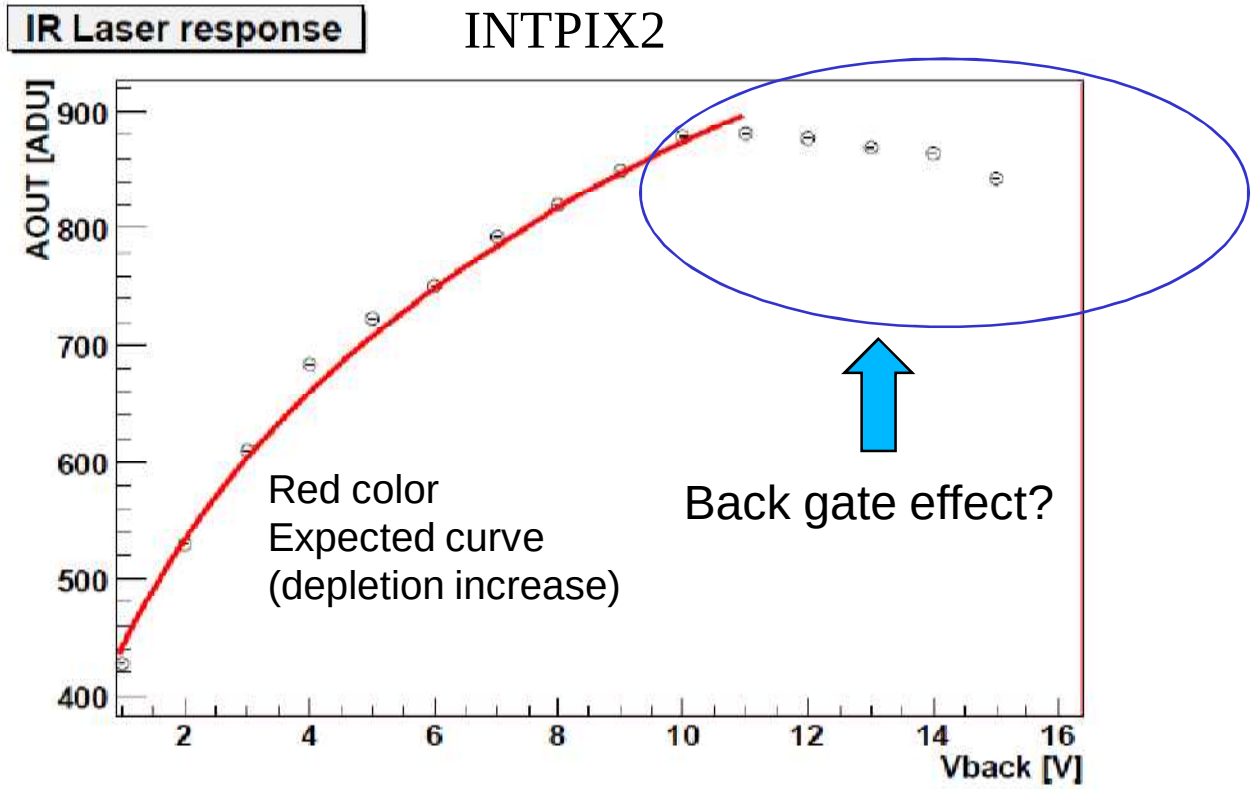
R&D issue and 3rd MPW run submitted on Feb. 09(FY08)





An example of R&D issue

Back bias voltage(recommended) 5V
(maximum operation voltage ~60V)
Why?
IR(980nm) response



R&D issues

Sensor and Electronics are placed very near position (~200nm) in SOI pixel. This may cause following problems.

•Back Gate Effect : Electric field from sensor will change the transistor characteristics.

•Electric field in oxide may increase hole trap probability at Si-SiO_2 interface, and therefore may reduce radiation tolerance.

•There may be crosstalk between circuit and sensor node. (still under investigation)

Solutions

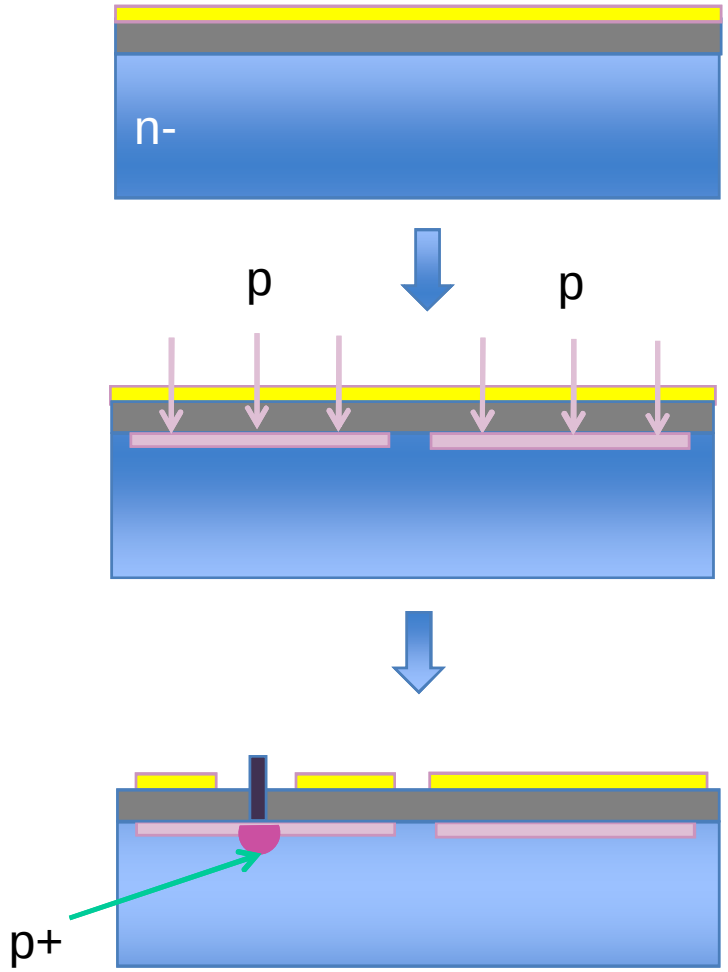
•Wafer Improvement : Double SOI Layer wafer, Higher Resistivity Wafer

•Process Improvement : Buried P-Well (BPW) process

•Integration Improvement : 3D vertical integration

Buried P-Well (BPW) Technology

Implant through SOI layer (Buried P-Well)



TCAD simulation

Process simulation by OKI

Device simulation by KEK

TiSSiEN

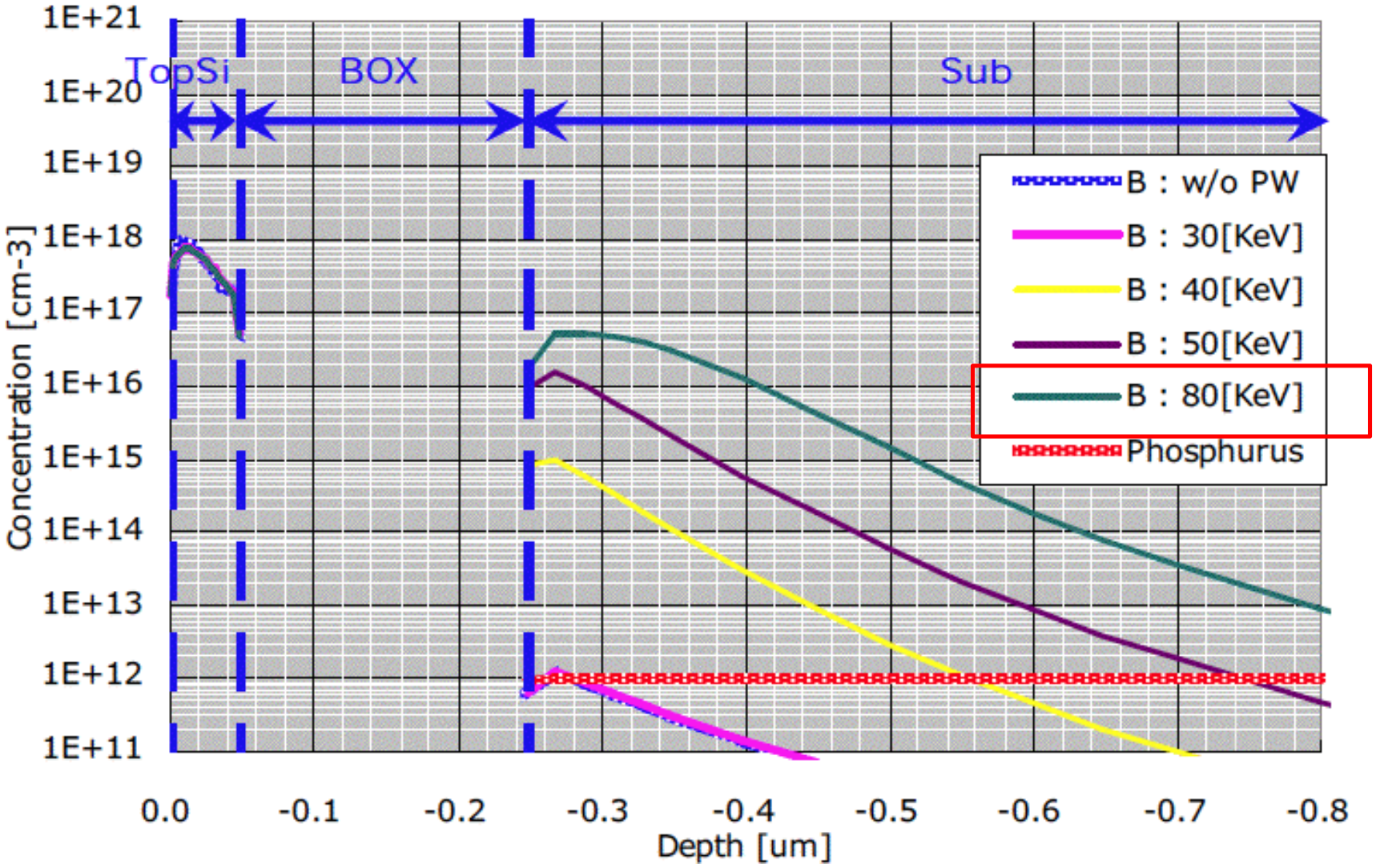
3D TCAD Simulator developed by SELETE Consortium Japan.

Currently TCAD international sells the software

http://www.tcad-international.com/english/index.html

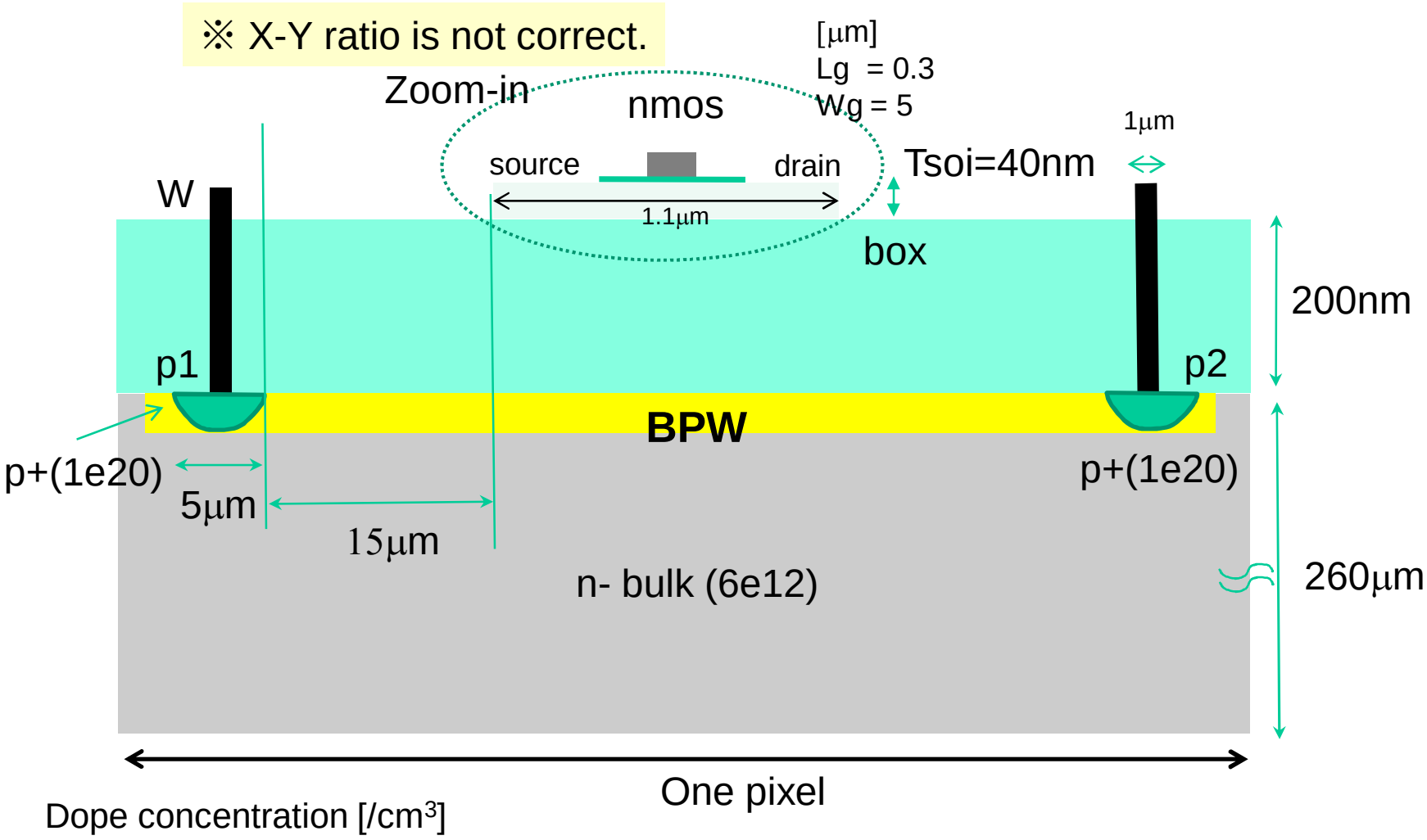
A simulation result by OKI

Concentration Profile of Implanted Dopant

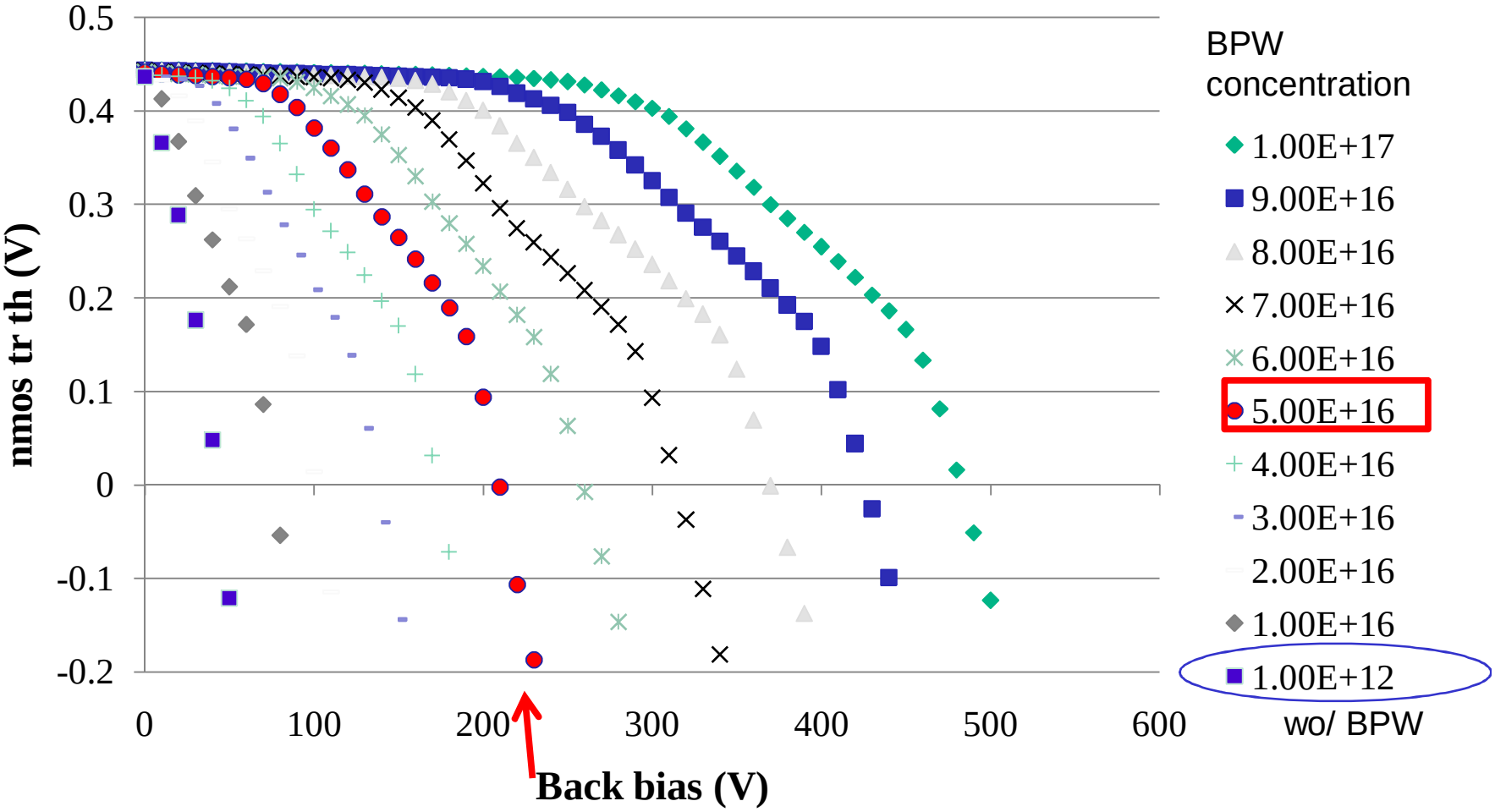


Device simulation by KEK

BPW simulation geometry

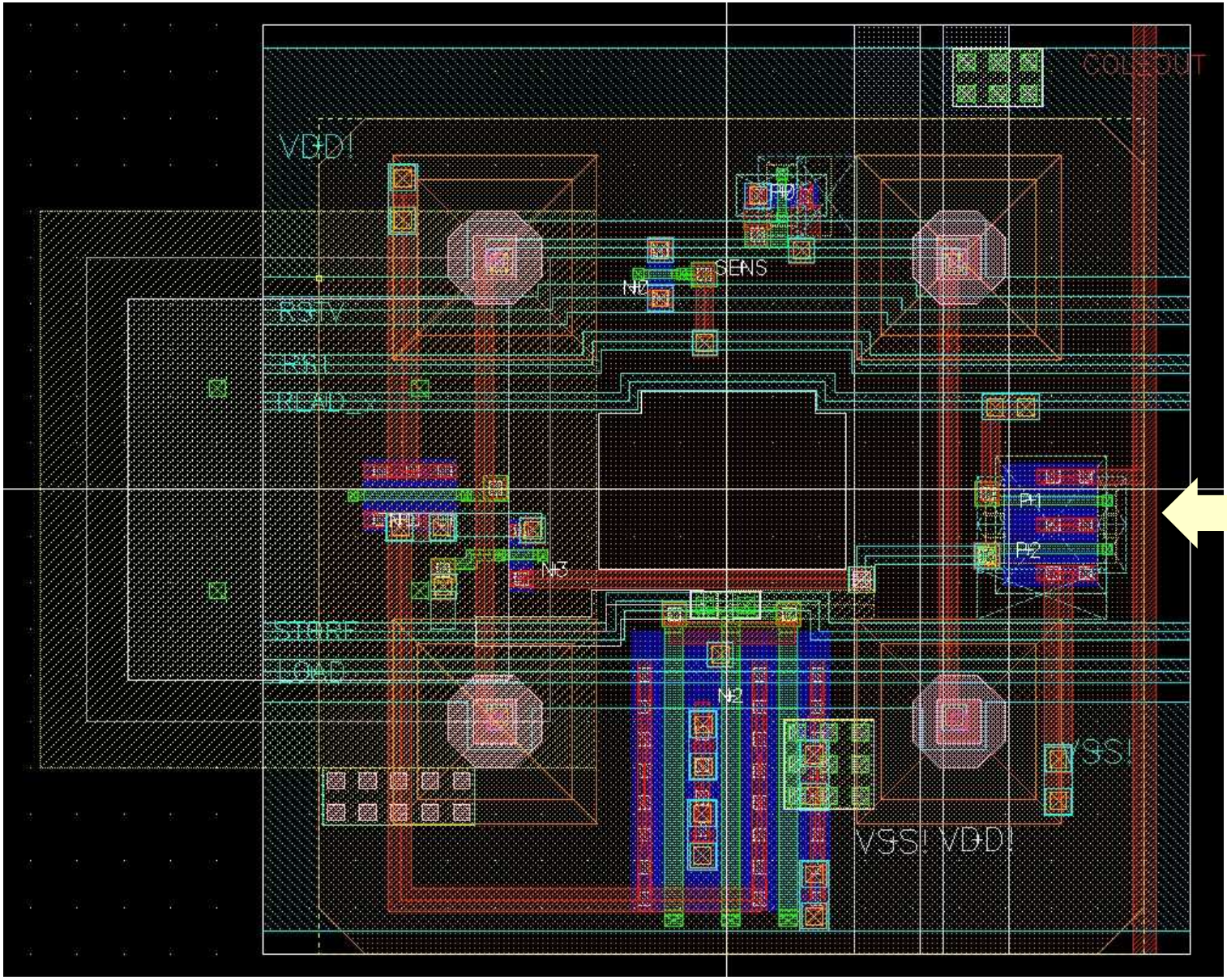


Device simulation result



Nmos tr. threshold doesn't decrease so much up to ~100V
OKI process simulation results are consistent with these results

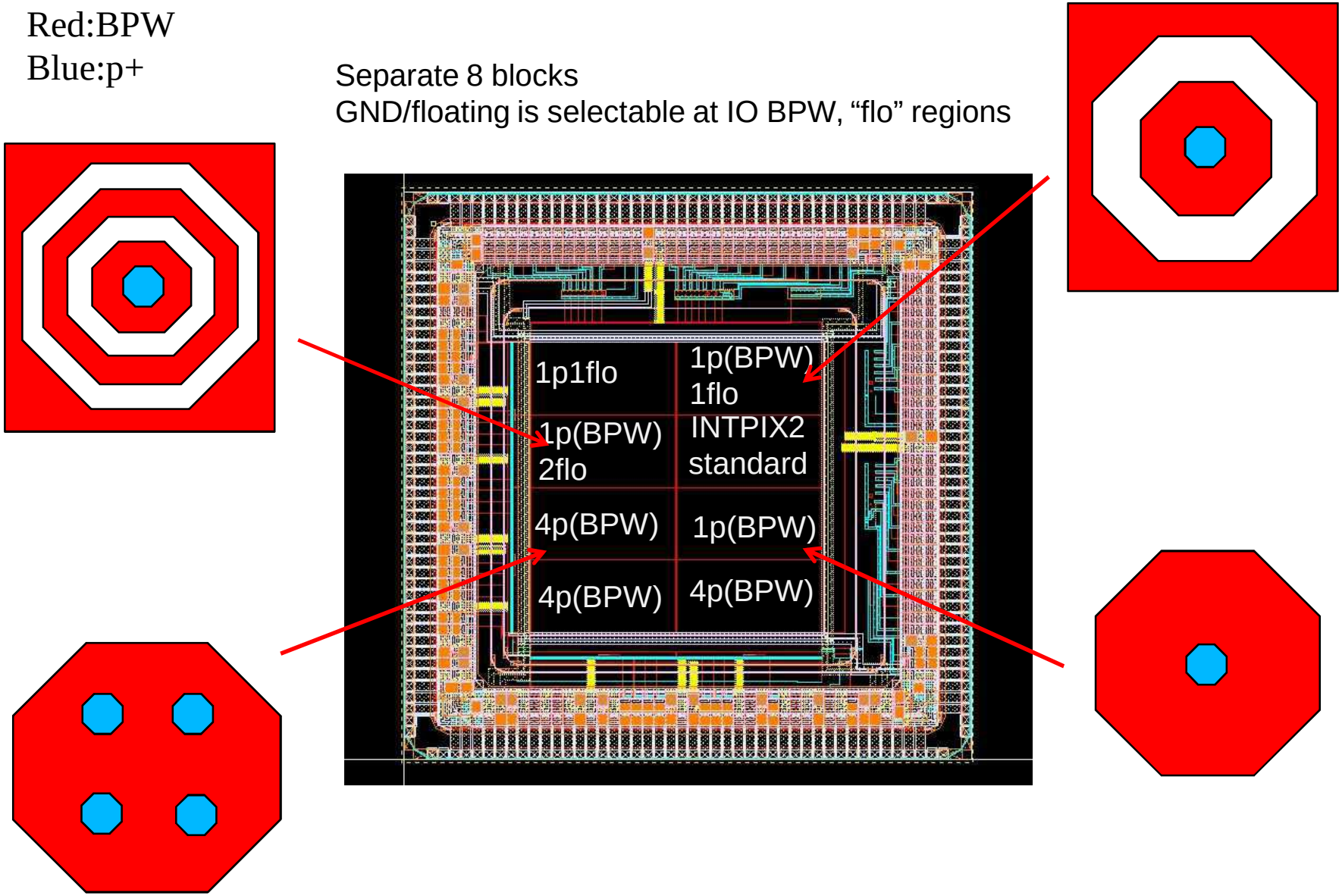
INTPIX3 structure (submitted in Feb. 2009)



INTPIX3 top layout

Pixel variation
Red:BPW
Blue:p+

Separate 8 blocks
GND/floating is selectable at IO BPW, “flo” regions



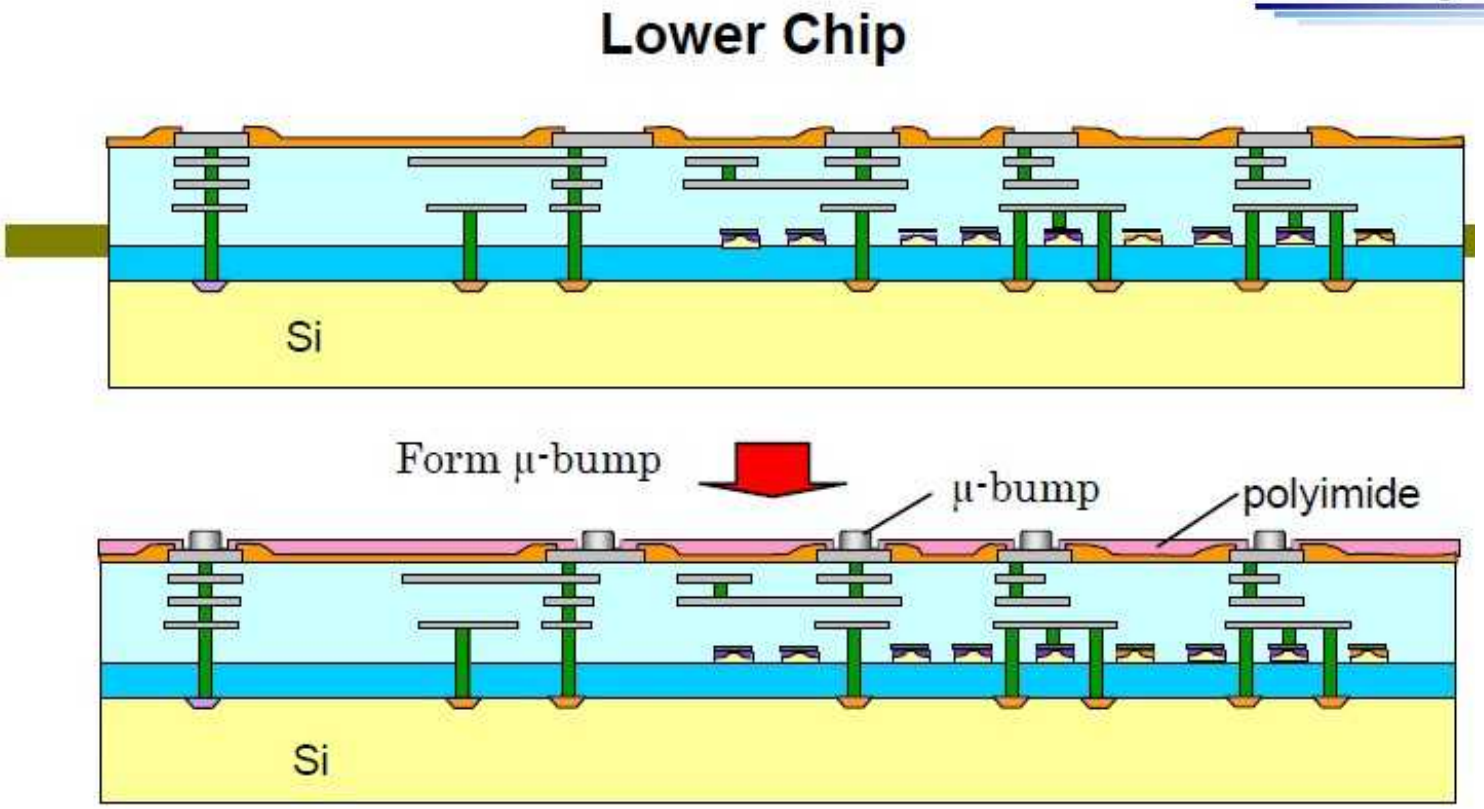
3D Vertical Integration

KEK/LBNL(Design) →OKI FY08 (process) → ZyCube (3D integration)

apply ZyCube μ-bump bonding (~5 um pitch) technique

1

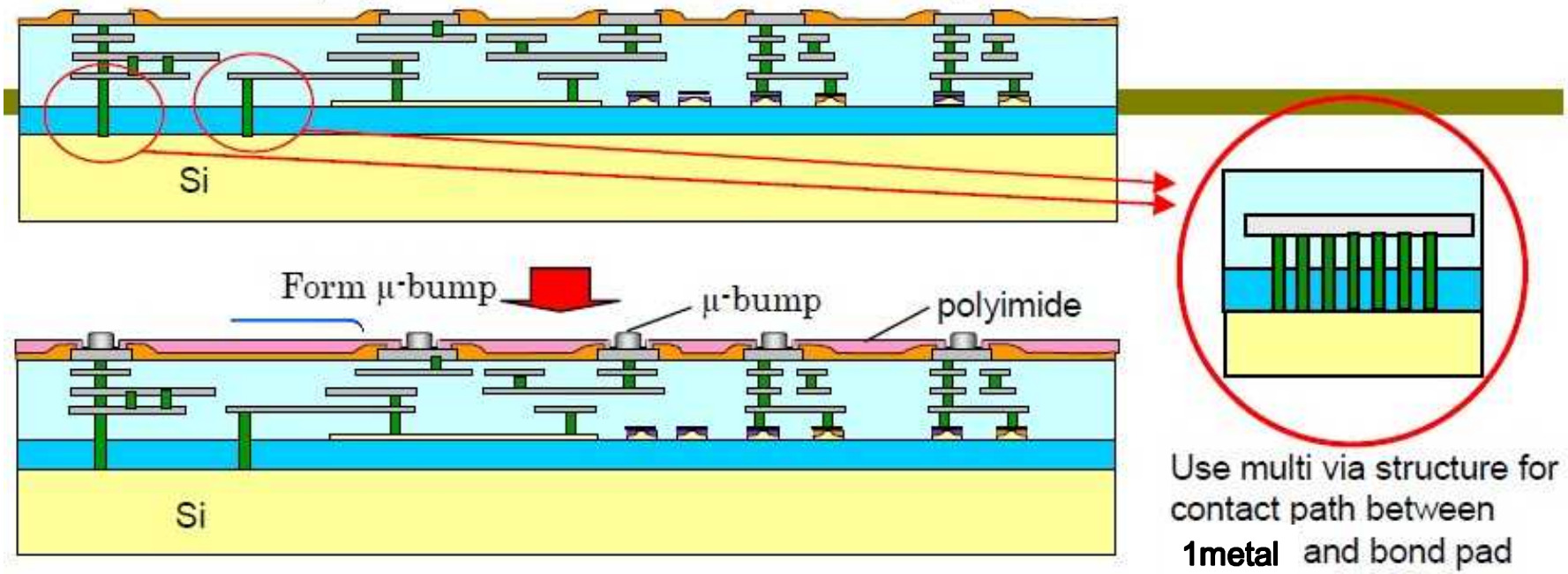
Stack Process Flow
(after finishing wafer process)



ザイキューブ
ZyCube

Upper Chip

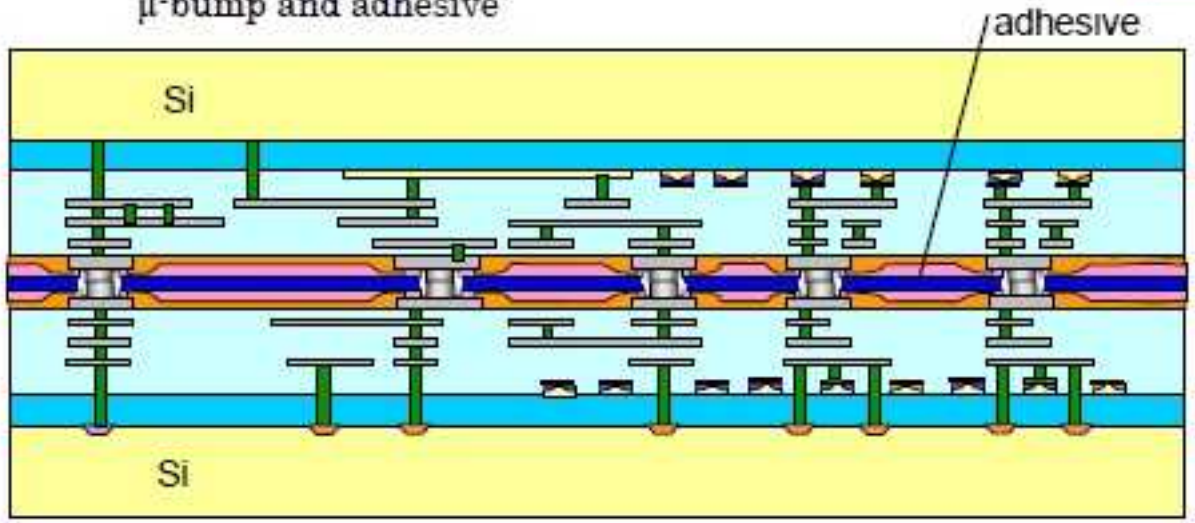
(Layout must be done with mirror inverted)



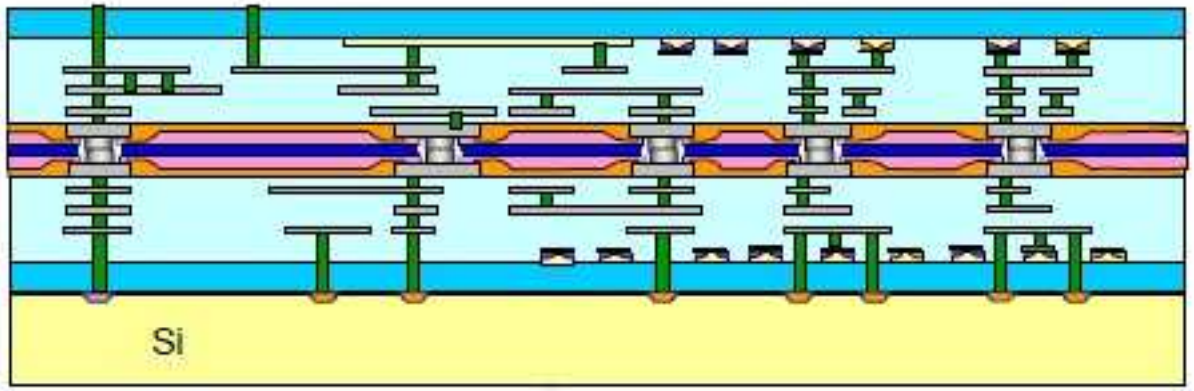
Use multi via structure for contact path between **1metal** and bond pad
dia./space 0.32/0.6μm
In left figure, single via is used for simplifying the cross section

ザイキューブ
ZyCube

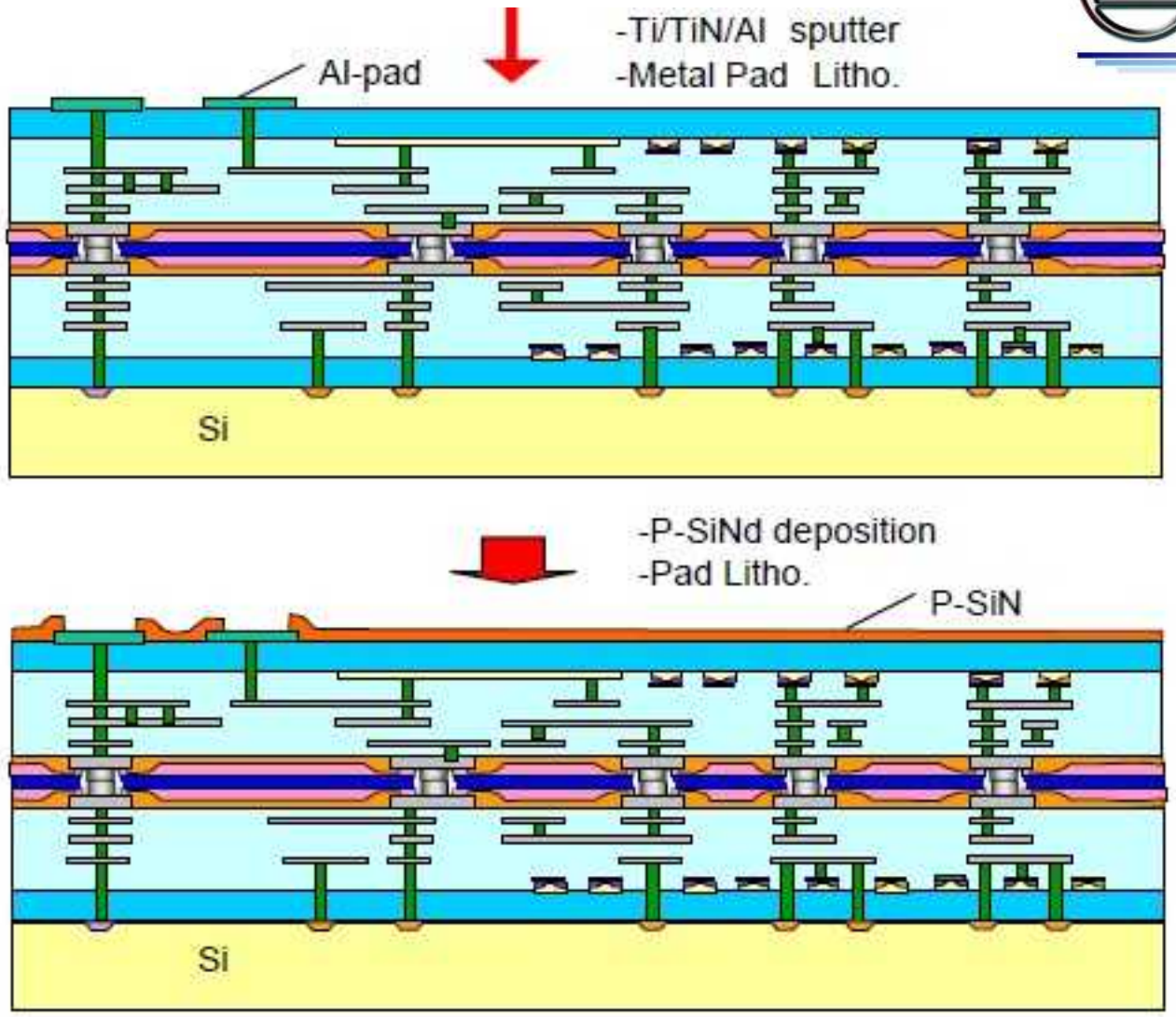
-Stack wafer with
μ-bump and adhesive



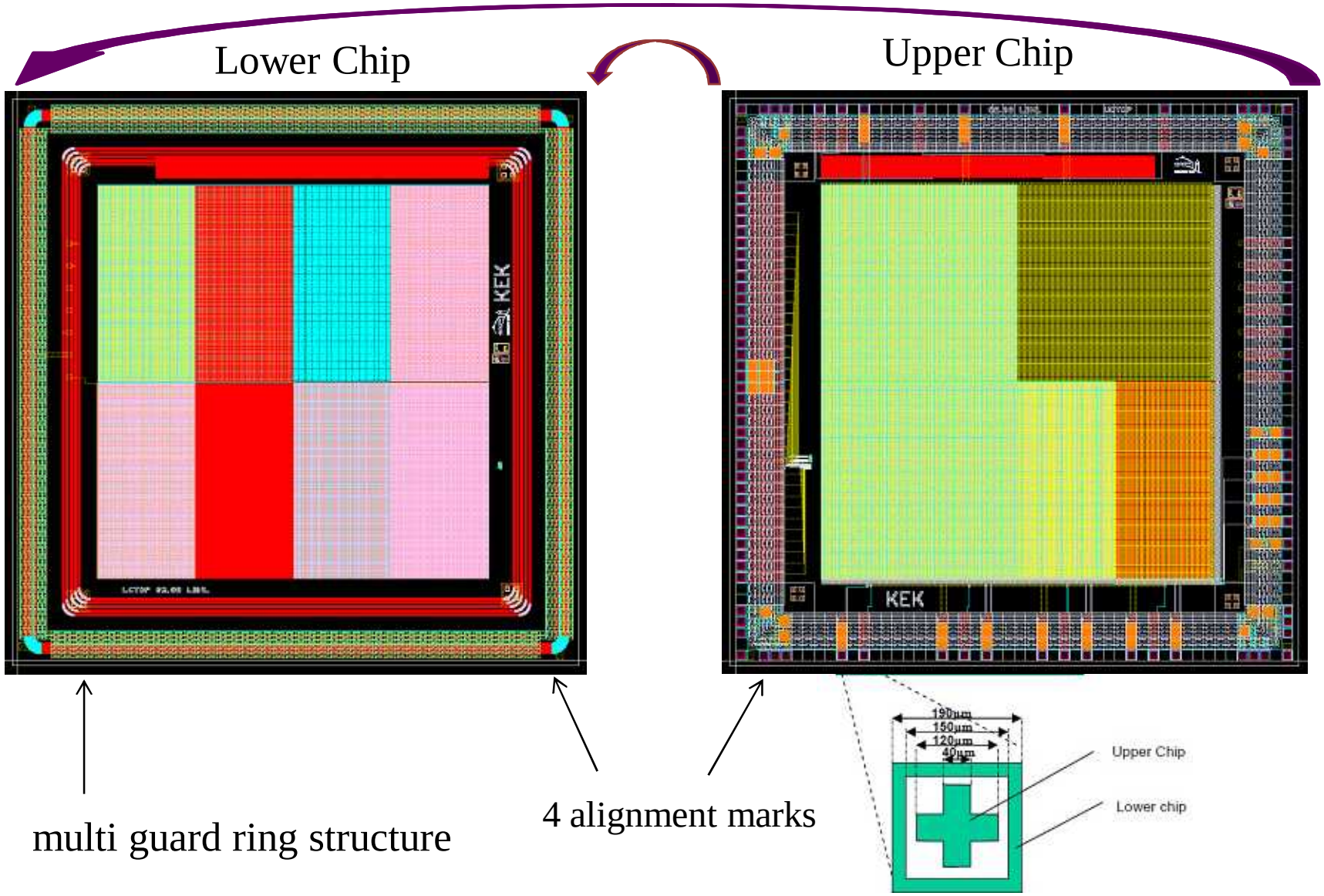
-Si etch
-SiO2 slight etch



ザイキューブ
ZyCube

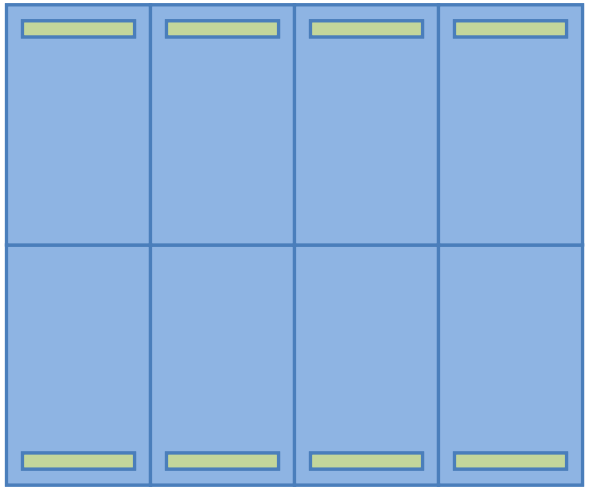


Two chip design by KEK/LBNL @ MPW FY08

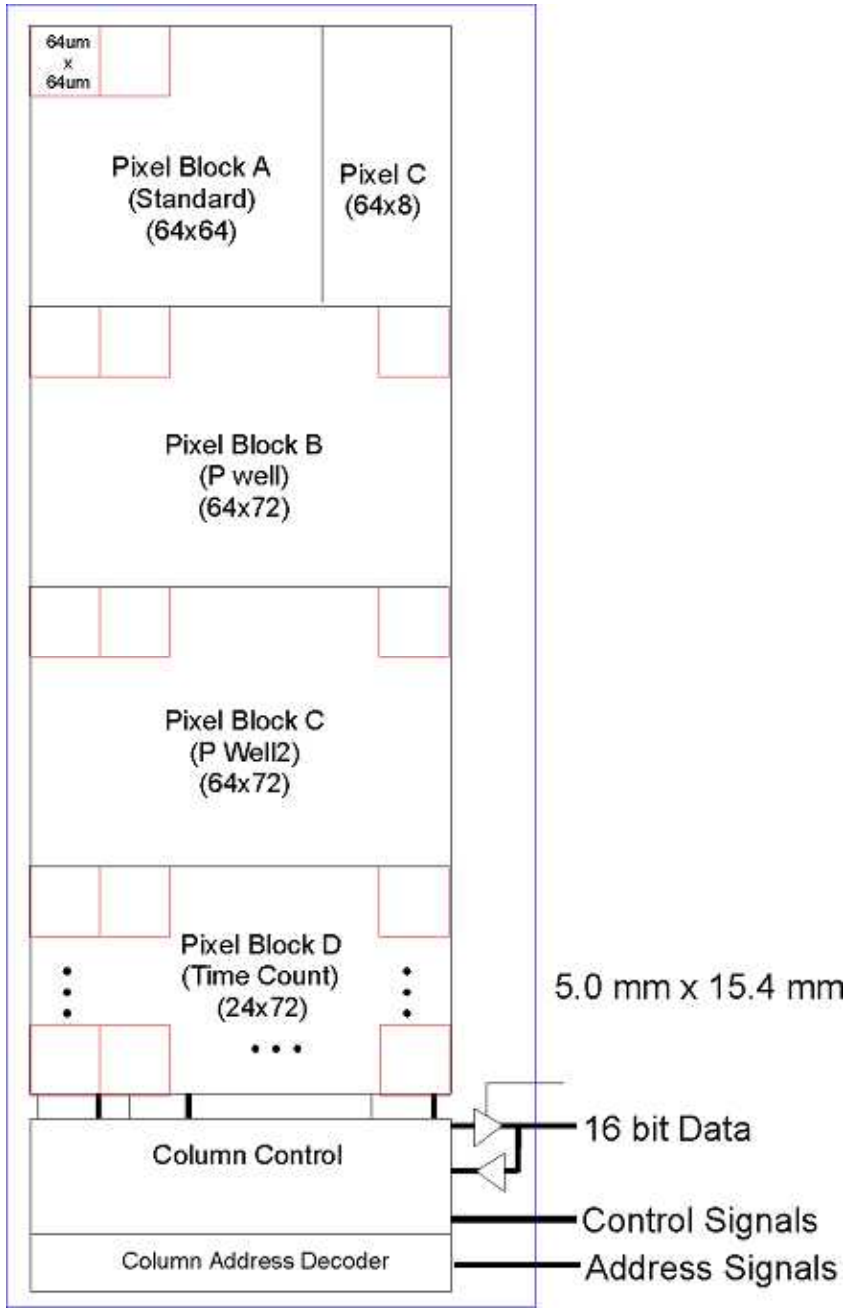


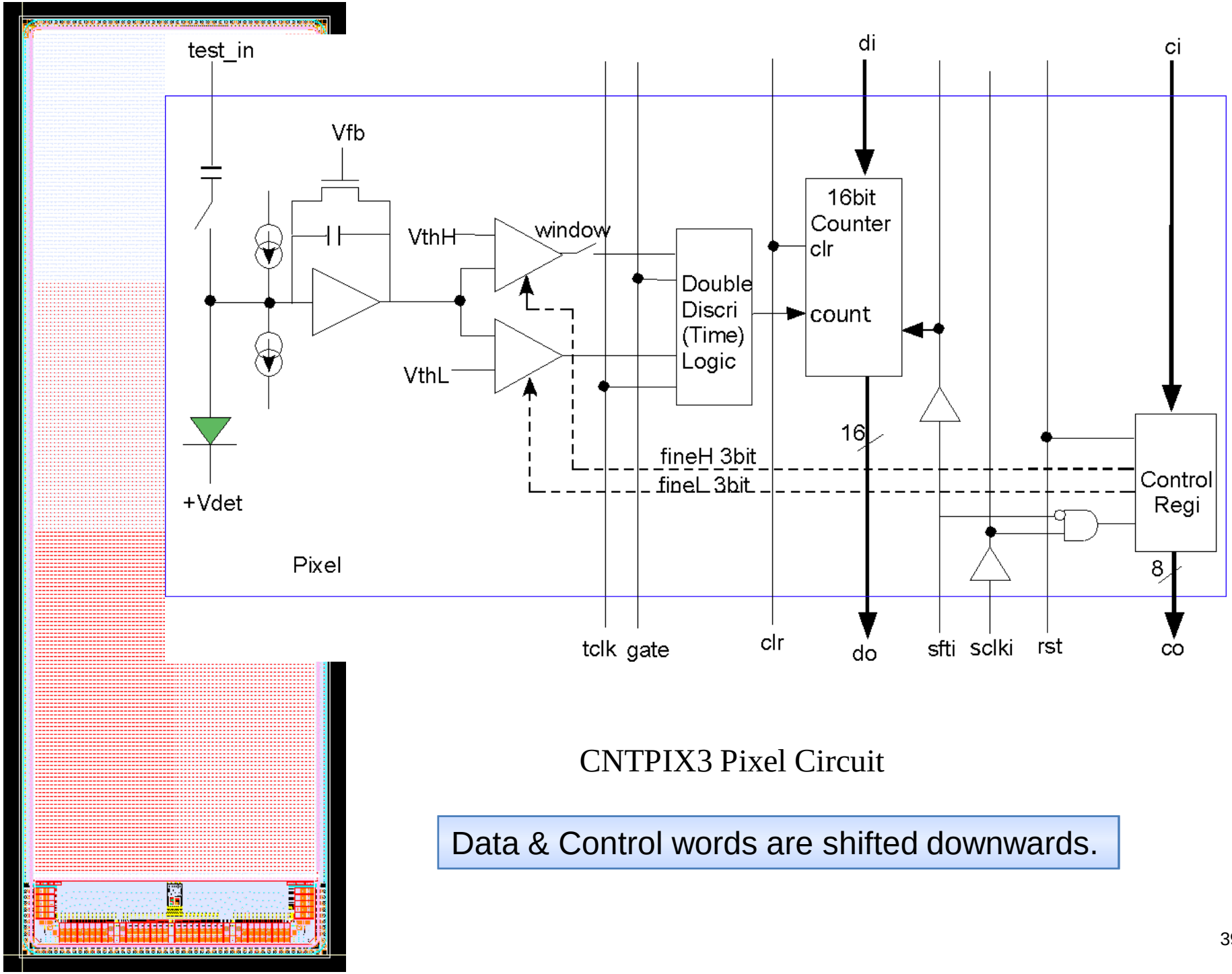
CNTPIX3

- 4 kinds of Pixel Block 72x216(15,552) pixels.
- 5.0 x 15.4 mm^2 chip size
- 64 x 64 um^2 pixel size
- IO pads are located in one side for stitching.



stitching





CNTPIX3 Pixel Circuit

Data & Control words are shifted downwards.

Summary

- SOI Pixel technology has many good features such as high speed, low material, high resolution ...
- We have confirmed good sensitivity of the SOI pixel detectors to Light and X-rays.
- We have already done 3 MPW runs from 2006, Each includes ~17 designs from many institutes.
- To improve the performance we are developing new techniques of 'Buried P-Well', and '3D Vertical Integration' .

Schedule

'05. 7: Start Collaboration with OKI Elec. Co. Ltd.

'05.10: TEG submission to OKI SOI 0.15 um process.

'06.12: 1st 0.15 um MPW run hosted by KEK.

'07.6: Process (and Fab.) is changed from 0.15 um to 0.2 um.

'08.1: 1st 0.2 um (FY07) MPW run was submitted.

'09.2: 2nd 0.2 um (FY08) MPW run was submitted.

‘09 5 (end) : FY08 process will ends → ’09 6 chip test

‘09 5 (end) : some wafers transfer to ZyCube →FY08 3D integration

'09.7 (end) : 3rd 0.2um (FY09A) MPW run deadline

‘09.10- : SR X-ray test @ KEK-PF

‘10.1? : 4th 0.2um (FY09B) MPW run is planned.

We welcome anyone who has interests in the SOI pixel technology to join the SOI MPW runs.

http://rd.kek.jp/project/soi/

SOI Pixel Collaboration

KEK : Y. Arai, Y. Unno, S. Terada, Y. Ikegami, T. Tsuboyama, T. Kohriki, Y. Ikemoto, T. Miyoshi, K. Tauchi, R. Ichimiya
Tsukuba Univ. : K. Hara, H. Miyake, T. Sega, M. Kochiyama
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Tohoku Univ. : Y. Onuki, H. Yamamoto, Y. Horii
Kyoto Univ. : T. Tsuru, H. Matsumoto
Kyoto Univ. of Education: R. Takashima, A. Takeda
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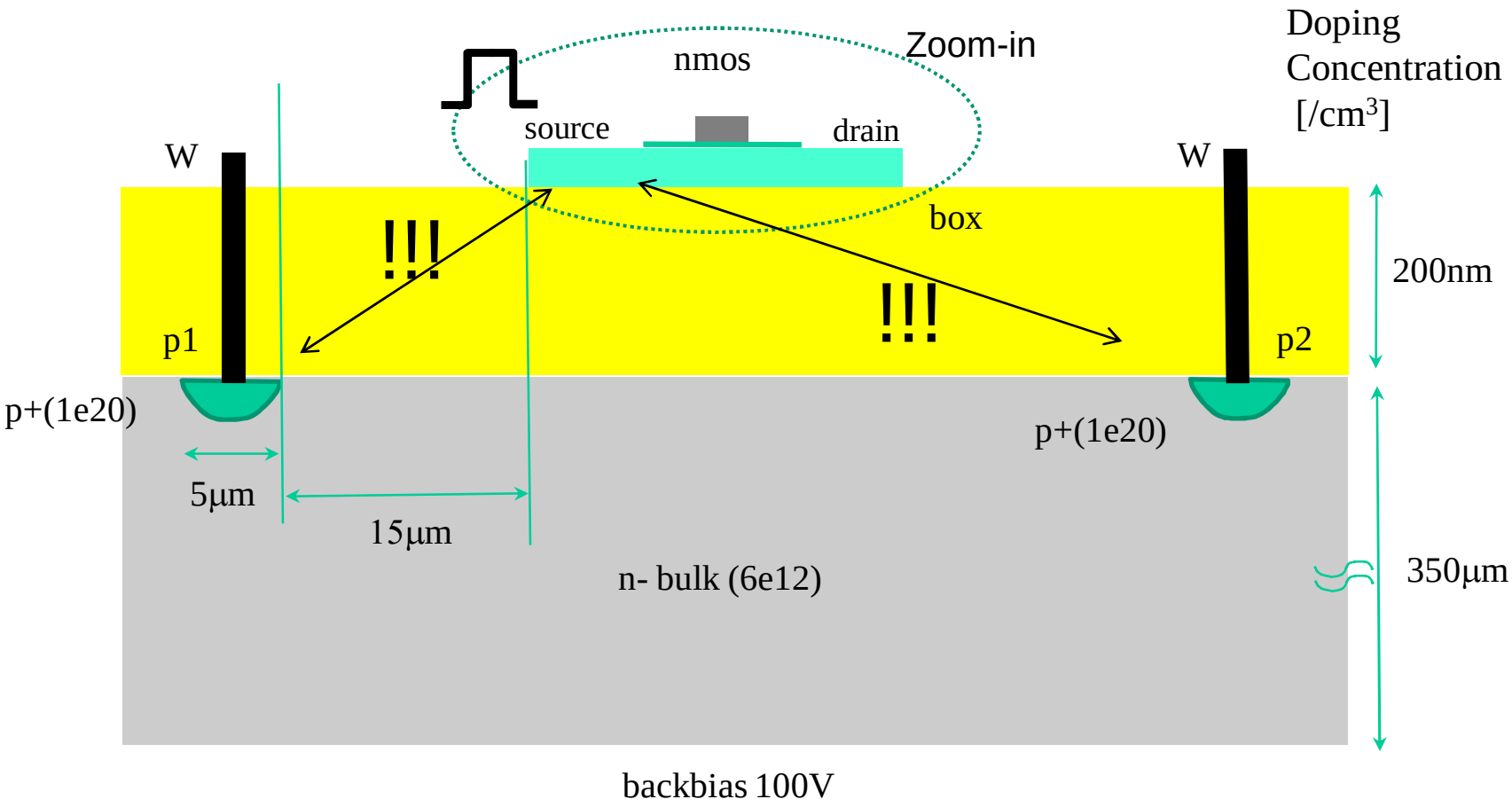
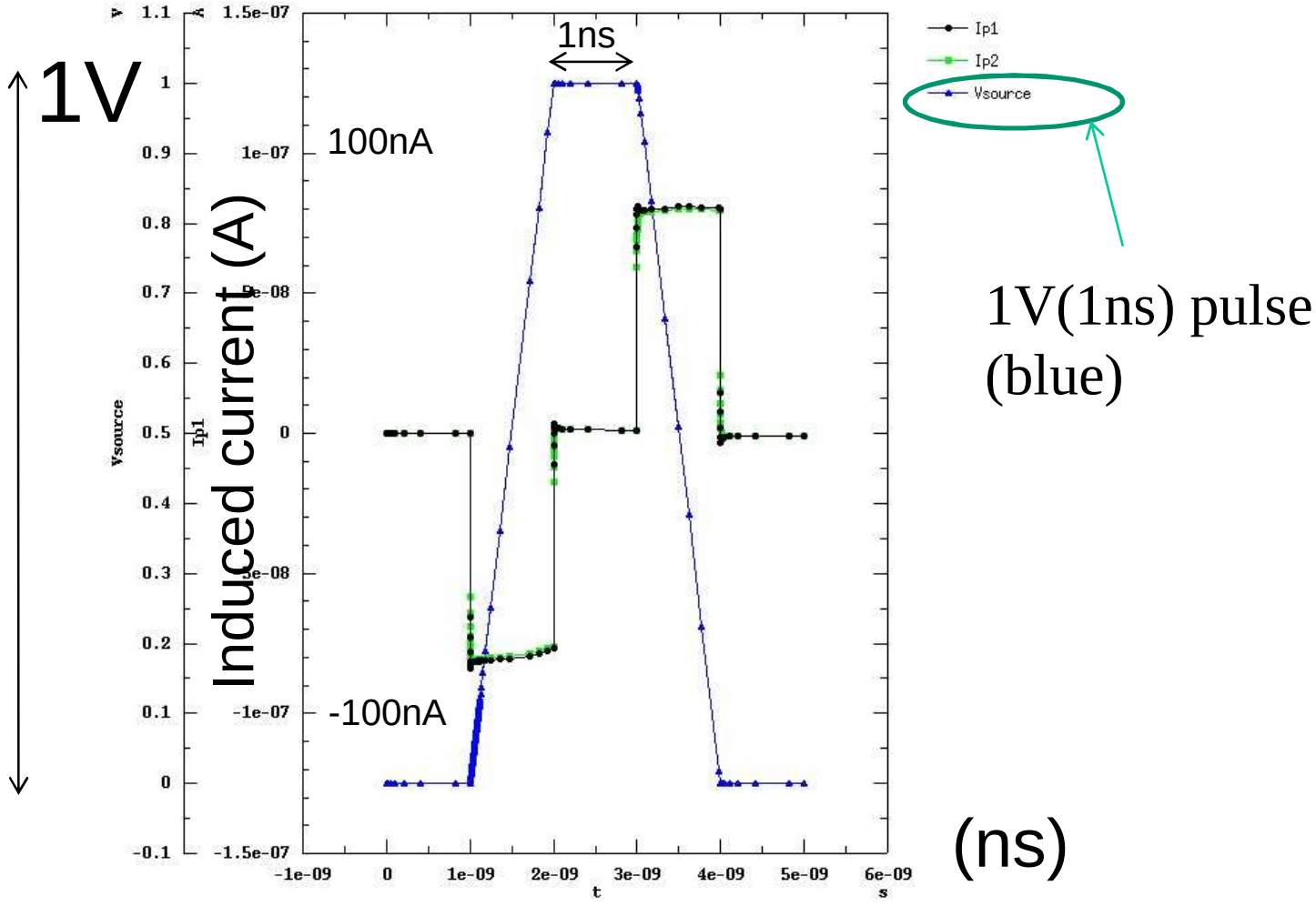
RIKEN : T. Hatsui, T. Kudo, T. Hirono, M. Yabashi, Y. Furukawa, A. Taketani
Hawaii: G. Varner, M. Cooney, H. Hoedlmoser, J. Kennedy, HB Sahoo
LBNL : M. Battaglia, P. Denes, C. Vu, D. Contarato, P. Giubilato, L. Glesener
FNAL : R. Yarema, R. Lipton, G. Deptuch, M. Trimpl
Krakow: P. Kapusta, H. Palka
INFN Padova: D. Bisello, S. Mattiazzo, D. Pantano
OKI Semiconductor Co. Ltd. : M. Ohno, K. Fukuda, H. Komatsubara, J. Ida, M. Okihara, H. Hayashi, Y. Kawai , A. Ohtomo

Supplements

On-going Simulation －crosstalk－



Crosstalk between MOS and sensor node



Currents induced differentially
Depends on distance between nmos and sensor node ((should be longer)
More real configuration has to be simulated
How to confirm?